ComputerCraft Magazine's Guide to Classic Eight-bit Microprocessors

You can find these microprocessors inside yesterday's computers, many of which are still in active use in schools, homes and small businesses. All were introduced in the 1970s. Many have found new life by being designed into modems, fax machines, disk controllers, EPROM programmers and other dedicated controllers

Prepared by Jan Axelson
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76 North Broadway, Hicksville, NY 11801

Intel 8085

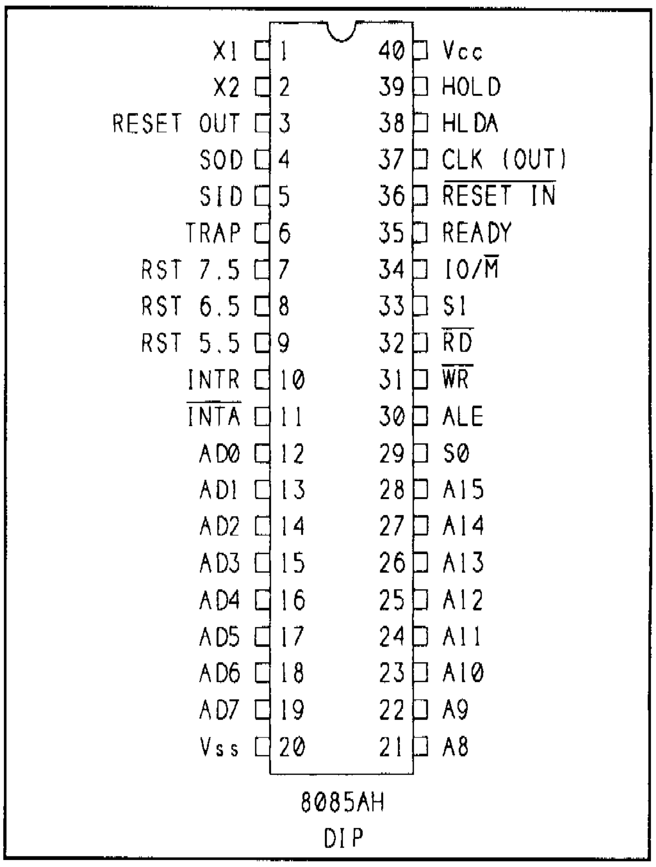
Summary

The 8085 is an enhanced version of the 8080, Intel's first eight-bit microprocessor. It executes all 8080 instructions and adds a clock generator, system controller, interrupt priorities and operation from a single +5-volt supply.

Features

Up to 6-MHz clock
Registers: two eight-bit, five 16-bit
Five external interrupts
113 instructions, four address modes
64K address space
Serial I/O system
CMOS version available

Pin	Function
1	Clock Generator Input 1
2	Clock Generator Input 2
3	Reset Output
4	Serial Output Data Line
5	Serial Input Data Line
6	Trap Interrupt, Non-maskable
7	Restart Interrupt 7.5
8	Restart Interrupt 6.5
9	Restart Interrupt 5.5
10	Interrupt Request
11	Interrupt Acknowledge
12	Address/Data Bit 0
13	Address/Data Bit 1
14	Address/Data Bit 2
15	Address/Data Bit 3
16	Address/Data Bit 4
17	Address/Data Bit 5
18	Address/Data Bit 6
19	Address/Data Bit 7
20	Circuit Ground
21	Address Bit 8
22	Address Bit 9
23	Address Bit 10
24	Address Bit 11
25	Address Bit 12
26	Address Bit 13
27	Address Bit 14
28	Address Bit 15
29	Machine Cycle Status 0
30	Address Latch Snable
31	Write Control
32	Read Control
33	Machine Cycle Status 1
34	I/O or Memory Select
35	Ready
36	Reset Input
37	Clock Output
38	Hold Acknowledge
39	Hold Bus
40	Power Supply



Manufacturer

Intel Literature
PO Box 7641
Mt. Prospect, IL 60056-7641
Tel.: 1-800-548-4725

Zilog Z80

Summary

The Z80 remains popular more than 15 years after its introduction. Like the 8085, it was designed as an enhanced 8080. Zilog offers many intelligent peripheral controller chips based on the Z80.

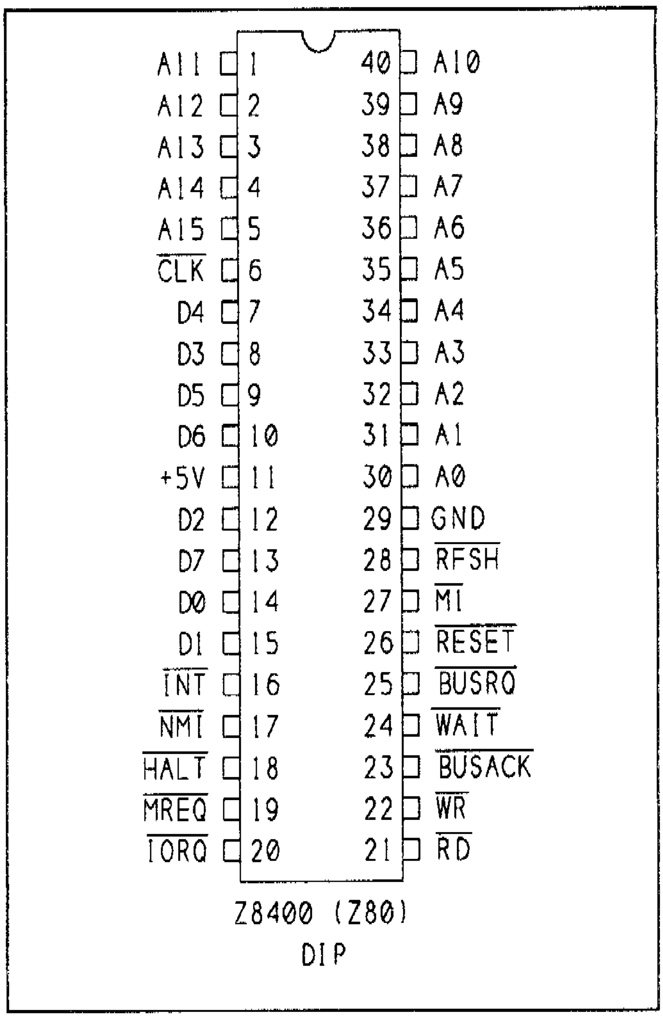
Features

Up to 20-MHz clock
Registers: 18 eight-bit, four 16-bit
Two interrupt sources
150 instructions, 10 address modes
64K address space
Block-transfer, block-search instructions

Family Members

Z8400	Basic Z80
Z8410	Direct-memory-access controller
Z8420	Parallel I/O controller
Z8430	Counter/timer controller
Z8440	Serial I/O controller

Zilog's Z80180 and Hitachi's 64180 add a memory management unit, DMA, UART, timers and other enhancements.
CMOS versions available (Z84C00, Z84C10, etc.)
Alternate packages include QFP, PLCC.



Z8400 (Z80)
DIP

Pin	Function
1	Address Bit 11
2	Address Bit 12
3	Address Bit 13
4	Address Bit 14
5	Address Bit 15
6	Clock Input
7	Data Bit 4
8	Data Bit 3
9	Data Bit 5
10	Data Bit 6
11	Power Supply
12	Data Bit 2
13	Data Bit 7
14	Data Bit 0
15	Data Bit 1
16	Interrupt Request
17	Non-Maskable Interrupt
18	Halt State Output
19	Memory request
20	I/O Request
21	Read
22	Write
23	Bus Acknowledge
24	Wait Input
25	Bus Request
26	Reset
27	Machine Cycle 1
28	Refresh Output
29	Ground
30	Address Bit 0
31	Address Bit 1
32	Address Bit 2
33	Address Bit 3
34	Address Bit 4
35	Address Bit 5
36	Address Bit 6
37	Address Bit 7
38	Address Bit 8
39	Address Bit 9
40	Address Bit 10

Manufacturers

Zilog, Inc.
210 E. Hacienda Ave.
Campbell, CA 95008-6609
Tel.: 408-370-8000

Hitachi America, Ltd.
Semiconductor and IC Div.
Hitachi Plaza, 2000 Sierra Point Pkwy.
Brisbane, CA 94005-1819
Tel.: 415-589-8300

Rockwell 6502

Summary

The Commodore VIC and Pet, Apple II and Atari 800/400 computers all were based on the 6502, and the Commodore 64 used a 6510 derivative of this chip, which is bus-compatible with Motorola's 6800.

Features

Up to 4-MHz clock
Six eight-bit registers
Two external interrupts
56 instructions, 13 address modes

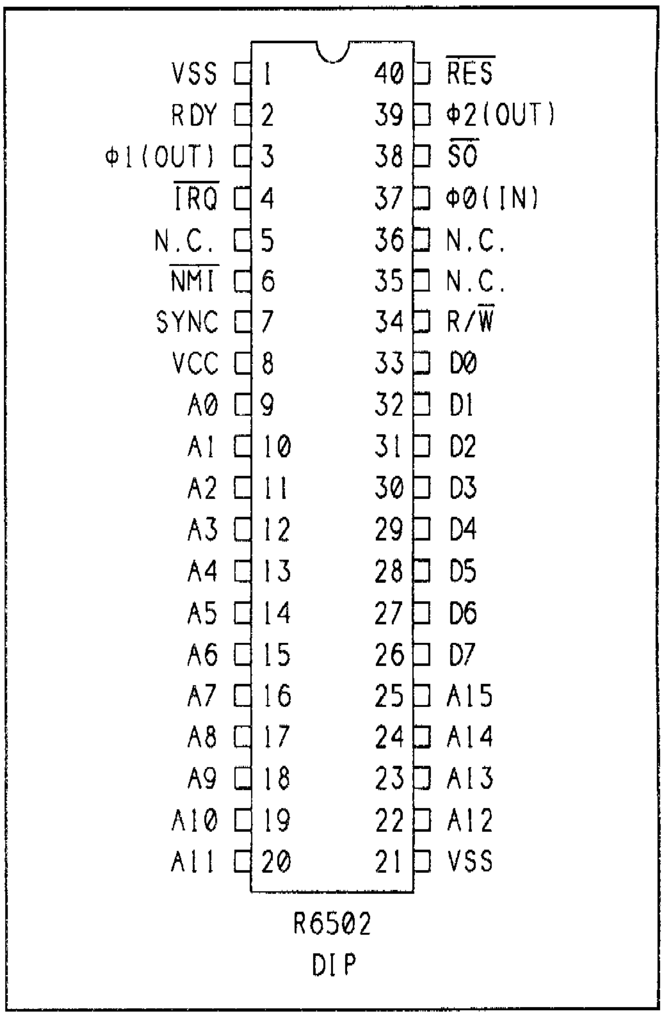
64K address space
Single instruction execution with SYNC output
Direct-memory-access capability

Family Members

6502	64K address space
6503	4K address space
6504	8K address space
6512	64K address space, external two-phase clock input

CMOS versions and PLCC package available

Pin	Function
1	Circuit Ground
2	Ready Input
3	Clock Generator Output 1
4	Interrupt Request
5	No Connection
6	Non-Maskable Interrupt
7	Sync Output
8	Supply Voltage
9	Address Bit 0
10	Address Bit 1
11	Address Bit 2
12	Address Bit 3
13	Address Bit 4
14	Address Bit 5
15	Address Bit 6
16	Address Bit 7
17	Address Bit 8
18	Address Bit 9
19	Address Bit 10
20	Address Bit 11
21	Circuit Ground
22	Address Bit 12
23	Address Bit 13
24	Address Bit 14
25	Address Bit 15
26	Data Bit 7
27	Data Bit 6
28	Data Bit 5
29	Data Bit 4
30	Data Bit 3
31	Data Bit 2
32	Data Bit 1
33	Data Bit 0
34	Read/Write
35	No Connection
36	No Connection
37	Clock Generator Input
38	Set Overflow Flag
39	Clock Generator Output 2
40	Reset



Manufacturers

Rockwell International
Digital Communications Div.
4311 Jamboree Rd.
Newport Beach, CA 92660
Tel.: 1-800-854-8099

Western Design Center
2166 E. Brown Rd.
Mesa, AZ 85213
Tel.: 602-962-4545

Harris CDP1802

Summary

The 1802 was the first CMOS microprocessor, introduced by RCA and now available from Harris. It includes a synchronous I/O interface.

Features

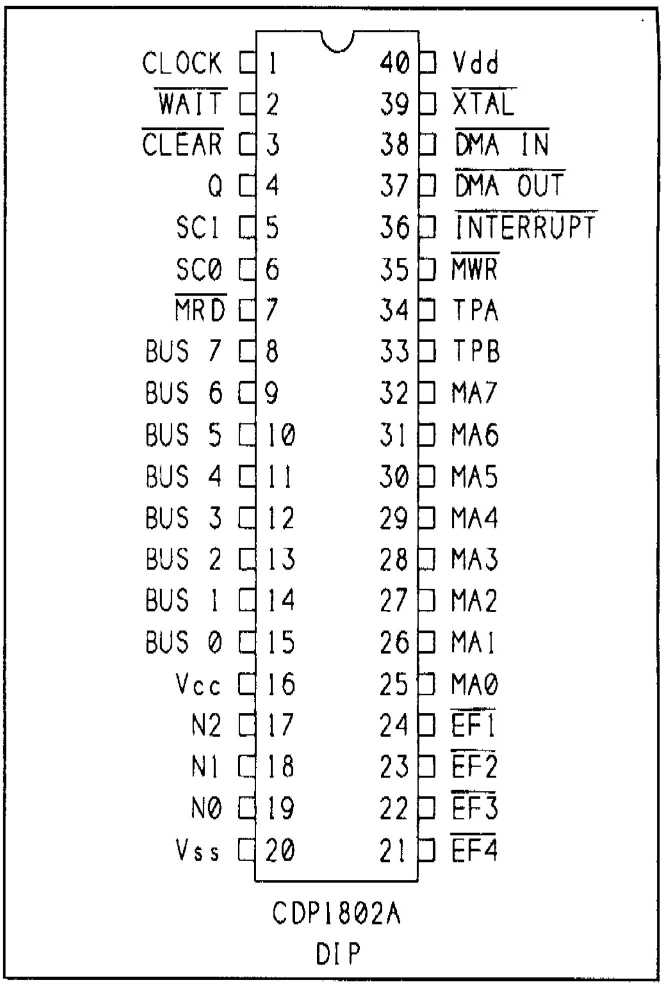
Up to 5-MHz clock
Registers: 16 16-bit, three eight-bit, four four-bit
One external interrupt
91 instructions
64K address space
Direct-memory-access capability

Family Members

CDP1802AC	3.2-MHz clock
CPD1802BC	5 MHz clock
CDP1805AC	5 MHz clock, 64 bytes of RAM, timer/counter, expanded instruction set PLCC package available

Pin	Function
1	Clock Input
2	Wait Control
3	Clear Control
4	Q Flip-Flop Output
5	CPU State Code 1
6	CPU State Code 0

7	Memory Read
8	Data Bus, Bit 7
9	Data Bus, Bit 6
10	Data Bus, Bit 5
11	Data Bus, Bit 4
12	Data Bus, Bit 3
13	Data Bus, Bit 2
14	Data Bus, Bit 1
15	Data Bus, Bit 0
16	I/O Voltage Supply
17	I/O Control Bit 2
18	I/O Control Bit 1
19	I/O Control Bit 0
20	Circuit Ground
21	Flag 4
22	Flag 3
23	Flag 2
24	Flag 1
25	Memory Address Bit 0
26	Memory Address Bit 1
27	Memory Address Bit 2
28	Memory Address Bit 3
29	Memory Address Bit 4
30	Memory Address Bit 5
31	Memory Address Bit 6
32	Memory Address Bit 7
33	Timing Pulse B
34	Timing Pulse A
35	Memory Write
36	Interrupt Request
37	Direct Memory Access Output
38	Direct Memory Access Input
39	Crystal
40	Internal Voltage Supply



Manufacturer

Harris Semiconductor
PO Box 883
Melbourne, FL 32901
Tel.: 407-724-7800

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Corrections

March 1993 Disk Drive Interfaces section transpose the two cable drawings on the first page with those on the second page.

ComputerCraft Magazine's PC & Microcontroller Data Guide

In this fifth installment of our special pull-out series, we continue with Microchip's PIC16C5x eight-bit microcontroller and move on to Intel's 8096 and Motorola's 68HC16 16-bit microcontrollers. Both of the latter two chips have 16-bit CPUs and are designed for applications in which programming complexity or the need for high speed make simpler eight-bit devices impractical.

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Microchip PIC16C5X

Summary

Devices in the CMOS PIC16C5X family are fast because they use 12-bit instructions, most of which require just one machine cycle to execute. All have user-programmable EPROM, either OTP (one-time-programmable) or UV-erasable. There are no external data/address buses, interrupt capabilities, or asynchronous serial port, although the new PIC17CXX series adds the last two of these. Digikey is a vendor.

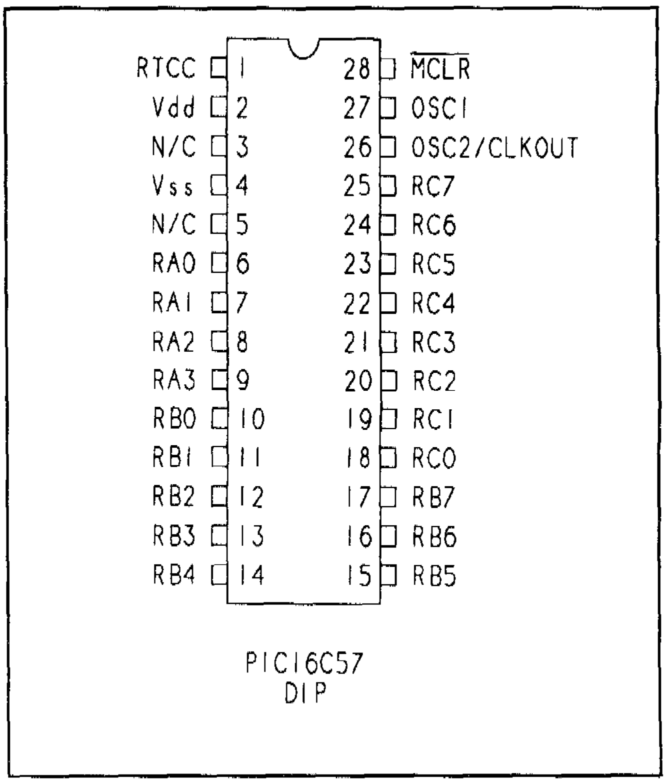
Features

Up to 2K x 12 of ROM
20-MHz clock
Up to 80 Registers
Up to 21 bits of I/O
Real-time clock, watchdog timer
33 instructions, three address modes
Four oscillator options, including low-cost and power-saving

Family Members

PIC16C57	2K x 12 of EPROM, 80 registers, 21 bits I/O
PIC16C54	512 x 12 of EPROM, 32 registers, 13 bits I/O
PIC16C55	512 x 12 of EPROM, 32 registers, 21 bits I/O
PIC16C56	1K x 12 of EPROM, 32 registers, 13 bits I/O

Packages include 18- to 28-pin DIPs and SOICs. Suffix -JW specifies UV-erasable EPROM.



Pin	Function
1	Real-time clock/calendar
2	Power supply
3	No connection
4	Ground
5	No connection
6	Port A, Bit 0
7	Port A, Bit 1
8	Port A, Bit 2
9	Port A, Bit 3
10	Port B, Bit 0
11	Port B, Bit 1
12	Port B, Bit 2
13	Port B, Bit 3
14	Port B, Bit 4
15	Port B, Bit 5
16	Port B, Bit 6
17	Port B, Bit 7

18	Port C, Bit 0
19	Port C, Bit 1
20	Port C, Bit 2
21	Port C, Bit 3
22	Port C, Bit 4
23	Port C, Bit 5
24	Port C, Bit 6
25	Port C, Bit 7
26	Oscillator Output/Clock Output
27	Oscillator Input
28	Master Clear

Manufacturer

Microchip Technology
2355 W. Chandler Blvd.
Chandler, AZ 85224-6199
Tel.: 602-963-7373

Intel 8X9X

Summary

The basic 8096 and other members of Intel's MCS-96 family are intended for high-speed control applications. Features include a 16-bit CPU and up to four 16-bit timers that can operate simultaneously. A high-speed I/O unit records the times of input triggers and triggers external events at specific times. EPROM variations can program themselves and others in auto, slave and run-time modes.

Features

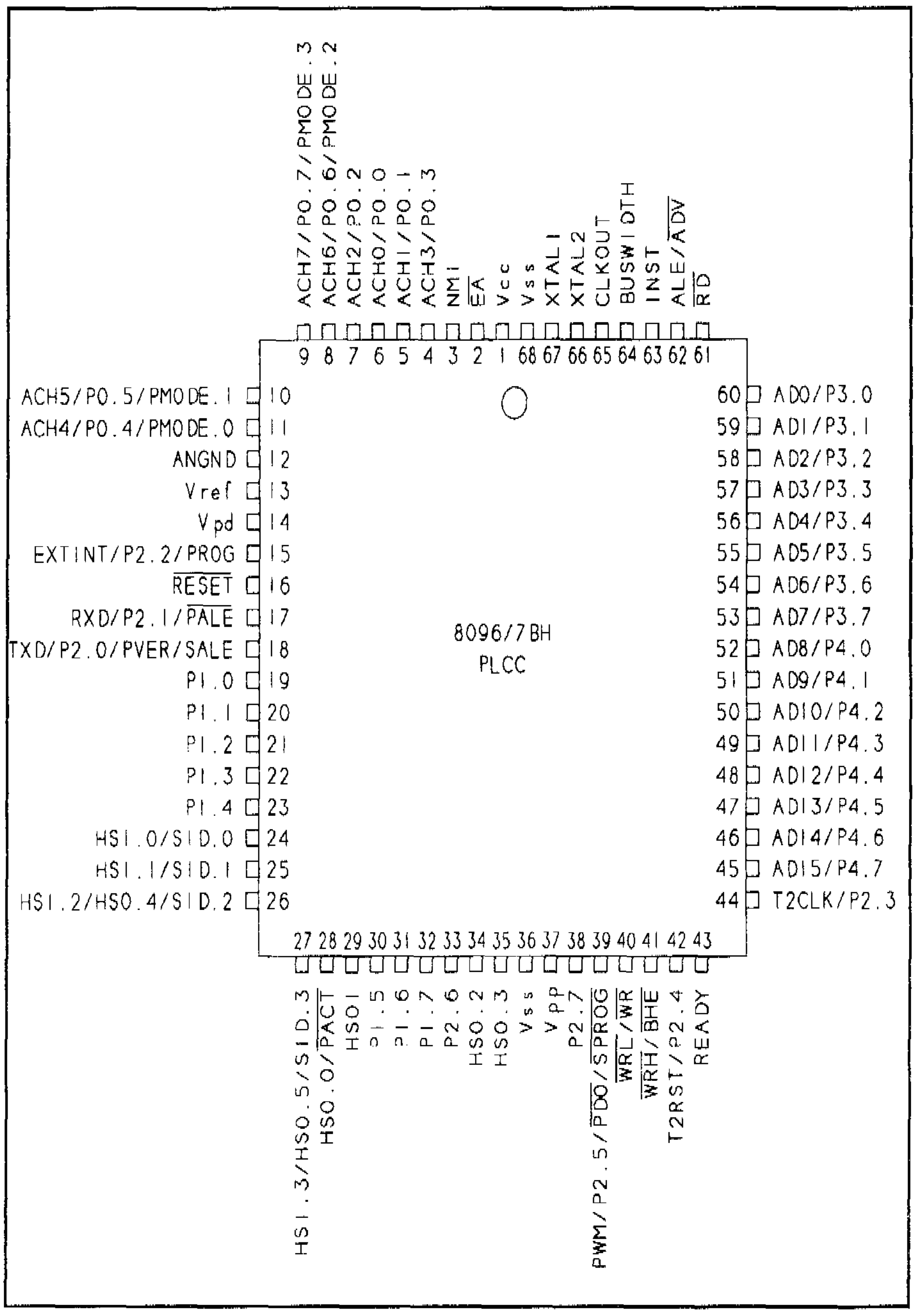
8K of ROM
232 bytes of RAM
20-MHz clock
232 registers
Serial port
20 interrupt sources, eight vectors
40 bits of I/O
Four 16-bit software timers
Two 16-bit counter/timers
Watchdog timer
10-bit A/D converter, eight channels
Pulse-width modulator output
73 instructions, six address modes

Family Members

8096BH	No ROM, 40 bits of I/O
8097BH	No ROM, 40 bits of I/O, A/D converter
8396BH	8K ROM, 40 bits of I/O
8395BH	8K ROM, 32 bits of I/O, A/D converter
8397BH	8K ROM, 32 bits of I/O, A/D converter
8796BH	8K EPROM, 40 bits of I/O
8795BH	8K EPROM, 32 bits of I/O, A/D converter
8797BH	8K EPROM, 40 bits of I/O, A/D converter

The 8XC196 devices are enhanced, high-performance members of the MCS-96 family. Alternativee packages include 48-pin DIP, 64-pin shrink DIP and 68-pin PGA.

Pin	Function
1	Supply Voltage
2	External Memory Access Enable
3	Non-Maskable Interrupt
4	Port 0, Bit 3; Analog Channel 3 (8x95/97)
5	Port 0, Bit 1; Analog Channel 1 (8x95/97)
6	Port 0, Bit 0; Analog Channel 0 (8x95/97)
7	Port 0, Bit 2; Analog Channel 2 (8x95/97)
8	Port 0, Bit 6; Analog Channel 6 (8x95/97); Program Mode Select 2 (879x)
9	Port 0, Bit 7; Analog Channel 7 (8x95/97); Program Mode Select 3 (879x)
10	Port 0, Bit 5; Analog Channel 5 (8x95/97); Program Mode Select 1 (879x)
11	Port 0, Bit 4; Analog Channel 4 (8x95/97); Program Mode Select 0 (879x)
12	Reference Ground for A/D Converter (8x95/97)
13	Reference Voltage for A/D Converter (8x95/97)
14	RAM Standby Supply Voltage
15	Port 2, Bit 2; External Interrupt; Program Pulse (879x)
16	Reset
17	Port 2, Bit 1; Serial Input Port; Program ALE (879x)
18	Port 2, Bit 0; Serial Output Port; Slave ALE (879x); Program Verify (879x)
19	Port 1, Bit 0
20	Port 1, Bit 1
21	Port 1, Bit 2
22	Port 1, Bit 3
23	Port 1, Bit 4



24	High-Speed Input 0; Slave ID 0 (879x)
25	High-Speed Input 1; Slave ID 1 (879x)
26	High-Speed Input 1; High-Speed Output 4; Slave ID 2 (879x)
27	High-Speed Input 3; High-Speed Output 5; Slave ID 3 (879x)
28	High-Speed Output 0; Programming Active (879x)
29	High-Speed Output 1
30	Port 1, Bit 5
31	Port 1, Bit 6
32	Port 1, Bit 7
33	Port 2, Bit 6
34	High-Speed Output 2
35	High-Speed Output 3
36	Digital Circuit Ground
37	EPROM Programming Voltage (879x)
38	Port 2, Bit 7
39	Port 2, Bit 5; Pulse-Width Modulator; Programming Duration Overflow (879x); Slave Program Pulse (879x)
40	Write to External Memory; Write Even Locations Only
41	Bus High Enable; Write Odd Locations Only
42	Port 2, Bit 4; Timer 2 Reset
43	Ready Input for Longer Bus Cycles
44	Port 2, Bit 3; Timer 2 Clock
45	Port 4, Bit 7; Address/Data Bit 15
46	Port 4, Bit 6; Address/Data Bit 14
47	Port 4, Bit 5; Address/Data Bit 13
48	Port 4, Bit 4; Address/Data Bit 12
49	Port 4, Bit 3; Address/Data Bit 11
50	Port 4, Bit 2; Address/Data Bit 10
51	Port 4, Bit 1; Address/Data Bit 9
52	Port 4, Bit 0; Address/Data Bit 8
53	Port 3, Bit 7; Address/Data Bit 7
54	Port 3, Bit 6; Address/Data Bit 6
55	Port 3, Bit 5; Address/Data Bit 5
56	Port 3, Bit 4; Address/Data Bit 4
57	Port 3, Bit 3; Address/Data Bit 3
58	Port 3, Bit 2; Address/Data Bit 2
59	Port 3, Bit 1; Address/Data Bit 1
60	Port 3, Bit 0; Address/Data Bit 0
61	Read External Memory
62	Address Latch Enable/Address Valid Output
63	Instruction Fetch Output
64	Bus Width Select
65	Clock Generator Output
66	Oscillator Inverter Output
67	Oscillator Inverter and Clock Generator Input
68	Digital Circuit Ground

Manufacturer

Intel Literature Sales
PO Box 7641
Mt. Prospect, IL 60056-7641
Tel.:1-800-548-4725

Motorola 68HC16

Summary

The 68HC16 has all of the resources of the eight-bit 68HC11, but with a 16-bit CPU and other additions. The chip can access 1M each of program and data memory. For digital signal-processing, there are dedicated registers for multiply and accumulate operations. Programmable chip-select pins provide address decoding for accessing blocks of memory.

Features

Up to 48K of ROM
Up to 2K of RAM
16.78-MHz clock
Registers: one 4-bit, two 8-bit, 11 16-bit and one 36-bit
QSPI (queued synchronous serial peripheral interface)
SCI (asynchronous serial communications interface)
207 interrupt vectors
Up to 79 bits I/O
Two 16-bit timers
261 instructions, 10 address modes
Eight- or 10-bit A/D converter
Two pulse width modulation outputs

Family Members

68HC16Z1	No ROM, 1K of RAM, 46 bits of I/O
68HC16Z2	8K of ROM, 2K of RAM, 46 bits of I/O
68HC16X1	32K of ROM, 2K of RAM, 2K of Flash EPROM, 67 bits ofI/O
68HC916X1	48K of Flash EPROM, 2K RAM, 2K Block of Flash EPROM, 67 bits of I/O
68HC16Y1	48K of ROM, 2K of RAM, 79 bits of I/O, eight channels of A/D, multi-channel communication interface, time processing unit

Pin	**Function**
1	Internal Module Power (Drain)
2	Internal Module Power (Source)
3	Output Compare 2/1; Port GP, Bit 4
4	Output Compare 1; Port GP, Bit 3
5	Input Capture 3; Port GP, Bit 2
6	Input Capture 2; Port GP, Bit 1
7	Input Capture 1; Port GP, Bit 0
8	External Periphery Power (Drain)
9	External Periphery Power (Source)
10	QSPI Master Input, Slave Output; Port QS, Bit 0
11	QSPI Master Output, Slave Input; Port QS, Bit 1
12	QSPI Serial Clock; Port QS, Bit 2
13	QSPI Peripheral Chip Select 0; Slave Select; Port QS, Bit 3
14	QSPI Peripheral Chip Select 1; Port QS, Bit 4
15	QSPI Peripheral Chip Select 2; Port QS, Bit 5
16	QSPI Peripheral Chip Select 3; Port QS, Bit 6
17	SCI Receive Data Input
18	SCI Transmit Data Output; Port QS, Bit 7
19	Address Bit 1
20	Address Bit 2
21	External Periphery Power (Drain)
22	External Periphery Power (Source)
23	Address Bit 3
24	Address Bit 4
25	Address Bit 5
26	Address Bit 6
27	Address Bit 7
28	Address Bit 8
29	Internal Module Power (Source)
30	Address Bit 9
31	Address Bit 10
32	Address Bit 11
33	Address Bit 12
34	Address Bit 13
35	Address Bit 14
36	Address Bit 15
37	Address Bit 16
38	Address Bit 17
39	Address Bit 18
40	External Periphery Power (Drain)
41	External Periphery Power (Source)

42 A/D Converter power (Drain)
43 A/D Converter power (Source)
44 ADC Analog Input 0; Port ADA, Bit 0
45 ADC Analog Input 1; Port ADA, Bit 1
46 ADC Analog Input 2; Port ADA, Bit 2
47 ADC Analog Input 3; Port ADA, Bit 3
48 ADC Analog Input 4; Port ADA, Bit 4
49 ADC Analog Input 5; Port ADA, Bit 5
50 High Reference Voltage
51 Low Reference Voltage
52 ADC Analog Input 6; Port ADA, Bit 6
53 ADC Analog Input 7; Port ADA, Bit 7
54 Standby Voltage
55 Crystal Driver
56 Clock Synthesizer Power
57 External Clock Input
58 Internal Module Power (Source)
59 Internal Module Power (Drain)
60 External Filter Capacitor
61 External Periphery Power (Drain)
62 External Periphery Power (Source)
63 System Clock Output
64 Freeze; Quotient Output
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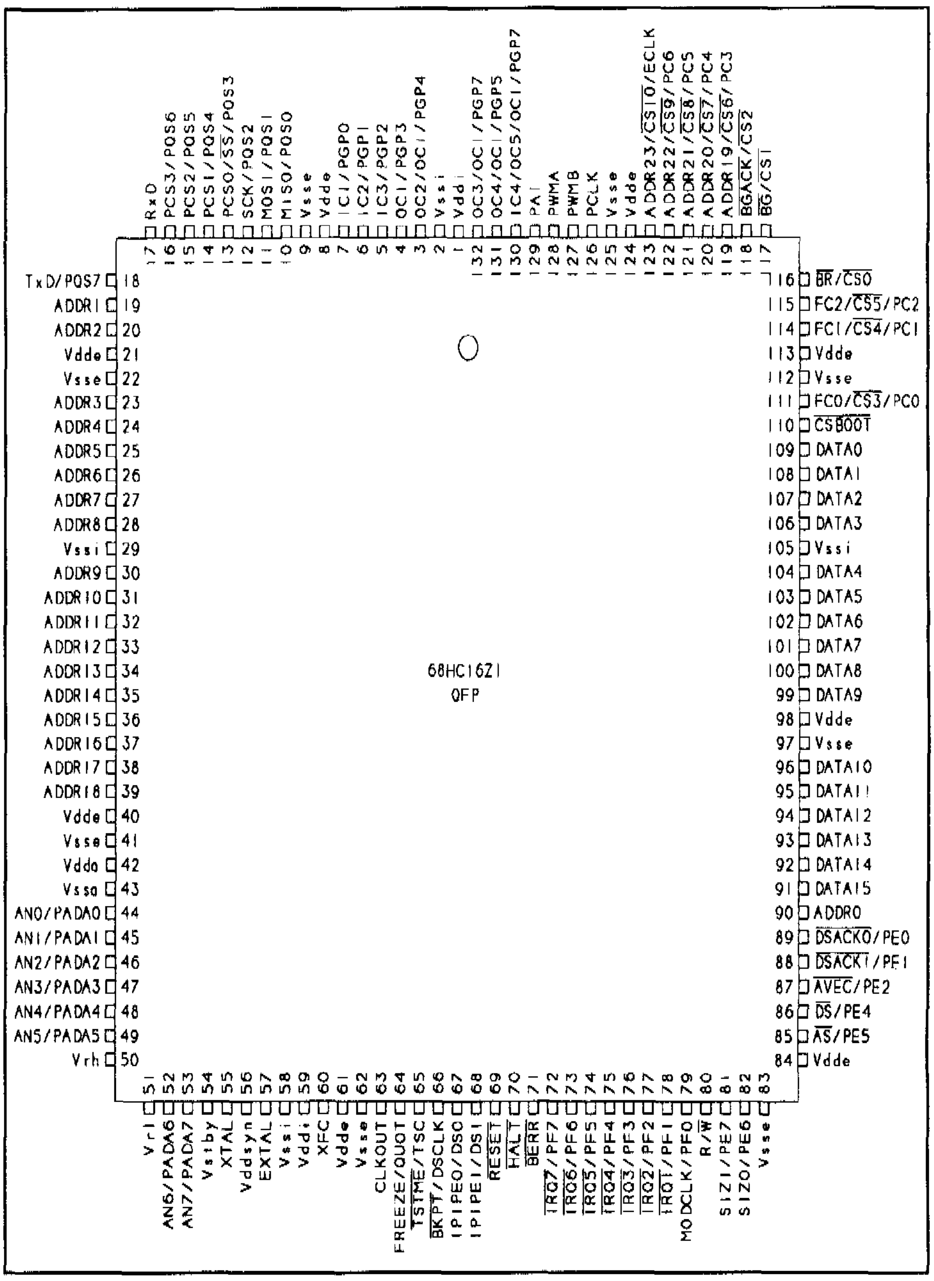
69 Reset
70 Halt External Bus Activity
71 Bus Error
72 Interrupt Request Level 7; Port F, Bit 7
73 Interrupt Request Level 6; Port F, Bit 6
74 Interrupt Request Level 5; Port F, Bit 5
75 Interrupt Request Level 4; Port F, Bit 4
76 Interrupt Request Level 3; Port F, Bit 3
77 Interrupt Request Level 2; Port F, Bit 2
78 Interrupt Request Level 1; Port F, Bit 1
79 Clock Mode Select; Port F, Bit 0
80 Read/Write Select
81 Size 1 (Indicates Bytes/bus Cycle); Port E, Bit 7
82 Size 0 (Indicates Bytes/bus Cycle); Port E, Bit 6
83 External Periphery Power (Source)
84 External Periphery Power (Drain)
85 Address Strobe; Port E, Bit 5
86 Data Strobe; Port E, Bit 4
87 Automatic Vector Request; Port E, Bit 2
88 Data and Size Acknowledge 1; Port E, Bit 1
89 Data and Size Acknowledge 0; Port E, Bit 0
90 Address Bit 0
91 Data Bit 15
92 Data Bit 14
93 Data Bit 13
94 Data Bit 12
95 Data Bit 11
96 Data Bit 10
97 External Periphery Power (Source)
98 External Periphery Power (Drain)
99 Data Bit 9
100 Data Bit 8
101 Data Bit 7
102 Data Bit 6
103 Data Bit 5
104 Data Bit 4
105 Internal Module Power (Source)
106 Data Bit 3
107 Data Bit 2
108 Data Bit 1
109 Data Bit 0
110 Boot Chip Select



111 Function Code 0; Chip Select 3; Port C, Bit 0
112 External Periphery Power (Source)
113 External Periphery Power (Drain)
114 Function Code 1; Chip Select 4; Port C, Bit 1
115 Function Code 2; Chip Select 5; Port C, Bit 2
116 Bus Request; Chip Select 0
117 Bus Grant; Chip Select 1
118 Bus Grant Acknowledge; Chip Select 2
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124 External Periphery Power (Drain)
125 External Periphery Power (Source)
126 Pulse Accumulator Clock
127 Pulse Width Modulator Output B
128 Pulse Width Modulator Output A
129 Pulse Accumulator Input
130 Input Capture 4; Output Compare 5/1; Port GP, Bit 7
131 Output Compare 4/1; Port GP, Bit 6
132 Output Compare 3/1; Port GP, Bit 5

Manufacturer

Motorola Semiconductor Products Inc.,
PO Box 20912
Phoenix, AZ 85036
Tel.: 1-800-521-6274

ComputerCraft Magazine's Guide to Popular Eight-Bit Microcontrollers

This month's pull-out section, the fourth in our series, has two uses. It's primary use is as a selection guide for comparing features of popular eight-bit microcontroller chips, while its secondary use is that it serves as a handy reference to device pinouts for testing and troubleshooting microcontroller devices. In coming months, we'll add to what appears here more eight- and 16-bit microcontrollers and significant details about them.

Prepared by Jan Axelson

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Intel 8051/52

Summary

The extremely popular 8051/52 family includes dozens of variations from Intel, Signetics/Philips, Siemens and others. The chip can access up to 64K bytes each of data and program memory. Low-cost development tools are widely available and include assemblers, compilers, simulators, monitor programs and circuit boards.

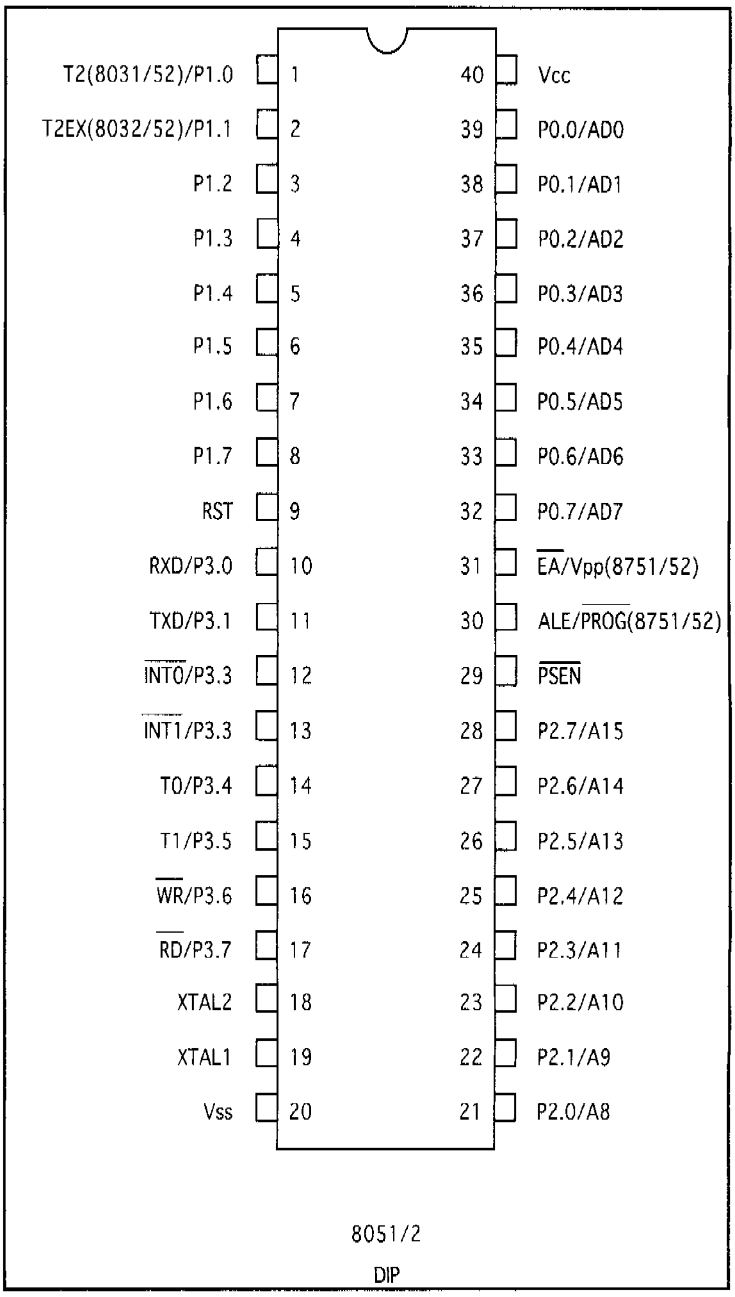
Features

Up to 32K of ROM
128 bytes of RAM (256 in 8032/52)
12-MHz clock (up to 40-MHz available)
Registers: 19 eight-bit, five 16-bit
Serial port
Five interrupt sources (six on 8032/52)
32 bits of I/O
Two 16-bit timers (three on 8032/52)
111 instructions, two address modes

Family Members

8051	4K of ROM, 128 of bytes of RAM, two timers
8052	8K of ROM, 256 bytes of RAM, three timers
8031	No of ROM, 128 bytes of RAM, two timers
8032	No of ROM, 256 bytes of RAM, three timers
8751	4K of EPROM, 128 bytes of RAM, two timers
8752	8K of EPROM, 256 bytes of RAM, three timers

80C51, 80C52, 80C31, etc. are CMOS versions of the above
80C51FA/B/C add more versatile timers and an enhanced serial channel
8052-BASIC has a BASIC interpreter in ROM
Alternative packages include 40-lead PLCC and 44-pin QFP



Pin	Function
1	Port 1, Bit 0 (also Timer 2 External Input on 8032/52)
2	Port 1, Bit 1 (also Timer 2 External Reload/Capture on 8032/52)
3	Port 1, Bit 2
4	Port 1, Bit 3
5	Port 1, Bit 4
6	Port 1, Bit 5
7	Port 1, Bit 6
8	Port 1, Bit 7
9	Reset
10	Port 3, Bit 0; Serial Input Port
11	Port 3, Bit 1; Serial Output Port
12	Port 3, Bit 2; External Interrupt 0
13	Port 3, Bit 3; External Interrupt 1
14	Port 3, Bit 4; Timer 0 External Input
15	Port 3, Bit 5; Timer 1 External Input
16	Port 3, Bit 5; Write Strobe for External Data Memory
17	Port 3, Bit 6; Read Strobe for External Data Memory
18	Input to Inverting Oscillator Amplifier
19	Output from Inverting Oscillator Amplifier
20	Circuit Ground
21	Port 2, Bit 0; Address Bit 8
22	Port 2, Bit 1; Address Bit 9
23	Port 2, Bit 2; Address Bit 10
24	Port 2, Bit 3; Address Bit 11
25	Port 2, Bit 4; Address Bit 12
26	Port 2, Bit 5; Address Bit 13
27	Port 2, Bit 6; Address Bit 14
28	Port 2, Bit 7; Address Bit 15
29	Program Store Enable: Read Strobe for External Program Memory
30	Address Latch Enable (also Program Pulse for 8751/8752)
31	External Access Enable for Program Memory (also Programming Voltage for 8751/8752)
32	Port 0, Bit 7; Address/Data Bit 7
33	Port 0, Bit 6; Address/Data Bit 6
34	Port 0, Bit 5; Address/Data Bit 5
35	Port 0, Bit 4; Address/Data Bit 4
36	Port 0, Bit 3; Address/Data Bit 3
37	Port 0, Bit 2; Address/Data Bit 2
38	Port 0, Bit 1; Address/Data Bit 1
39	Port 0, Bit 0; Address/Data Bit 0
40	Supply Voltage

Manufacturers

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 95051
Tel.: 408-765-8080

Philips Components/Signetics
811 E. Arques Ave., PO Box 3409
Sunnyvale, CA 94088
Tel.:408-991-2000

Siemens Components
2191 Laurelwood Rd.,
Santa Clara, CA 95054
Tel.: 408-980-4500

Motorola 68HC05

Summary

Because most 68HC05s can't access external memory, program and data memory must be on-chip. There are more than 100 variations, including tiny 16-pin devices. Motorola offers freeware assemblers, programming tools, and evaluation boards for project development. In 1991, more 68HC05s were sold than any other eight-bit microcontroller.

Features

Up to 16K of ROM
32 to 1.2K bytes of RAM
2.1-MHz bus speed
32 eight-bit registers
SCI (ansynchronous serial communications interface)
SPI (synchronous serial peripheral interface)
five interrupt sources
31 bits of I/O
One 16-bit timer
62 instructions, 10 address modes

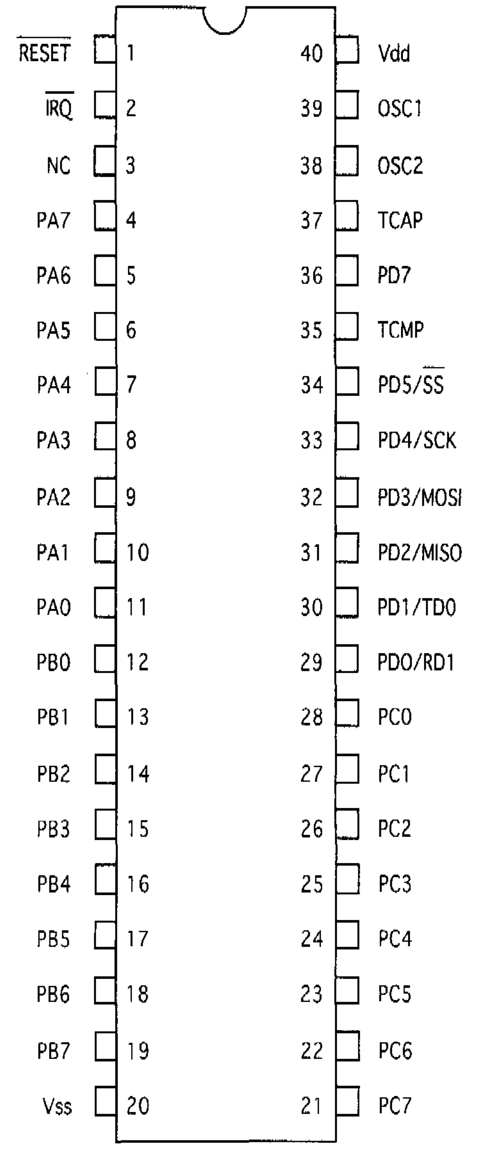
Family Members

MC68HC05C4	4K of ROM, 176 bytes of RAM, 31 bits I/O, SCI, SPI
MC68HC05C8	7.7K of ROM, 176 bytes of RAM, 31 bits I/O, SCI, SPI
MC68HC05C2	2K of ROM, 176 bytes of RAM, 31 bits I/O
MC68HC705C4	4K of EPROM, 176 bytes of RAM, 24 bits I/O, SCI, SPI
MC68HC705K1	504 bytes of EPROM, 64-bit personality EPROM, 32 bytes of RAM, 10 bits I/O, 16-pin DIP or SOIC

MC68HC05B4 adds an eight-channel analog-to-digital (A/D) converter, watchdog system and enhanced timers

6805 family is similar but uses HMOS (high-density n-channel MOS) technology, not CMOS PLCC package is also available

Pin	Function
1	Reset
2	External Interrupt Request
3	No Connection
4	Port A, Bit 7
5	Port A, Bit 6
6	Port A, Bit 5
7	Port A, Bit 4
8	Port A, Bit 3
9	Port A, Bit 2
10	Port A, Bit 1
11	Port A, Bit 0
12	Port B, Bit 0
13	Port B, Bit 1
14	Port B, Bit 2
15	Port B, Bit 3
16	Port B, Bit 4
17	Port B, Bit 5
18	Port B, Bit 6
19	Port B, Bit 7
20	Circuit Ground
21	Port C, Bit 7
22	Port C, Bit 6
23	Port C, Bit 5
24	Port C, Bit 4
25	Port C, Bit 3
26	Port C, Bit 2
27	Port C, Bit 1
28	Port C, Bit 0
29	Port D, Bit 0; SCI Receive Data Input
30	Port D, bit 1; SCI Transmit Data Output
31	Port D, bit 2; SPI Master Input/Slave Output
32	Port D, bit 3; SPI Master Output/Slave Input
33	Port D, bit 4; SPI Serial Clock
34	Port D, bit 5; SPI Slave Select
35	Timer Output Compare
36	Port D, Bit 7
37	Timer Input Capture
38	Oscillator 2 (Output)
39	Oscillator 1 (Input)
40	Supply Voltage



68HC05

DIP

Manufacturer

Motorola Semiconductor Products Inc.
PO Box 20912
Phoenix, AZ 85036
Tel.: 1-800-521-6274

Motorola 68HC11

Summary

The full-featured CMOS 68HC11 has on-chip EEPROM, flexible programmable timers and an eight-bit, eight-channel analog-to-digital (A/D) converter. Its instruction set is similar to that of the 68HC05 but is an expanded version. The chip can address 64K bytes of external memory. Motorola offers many variations, freeware assemblers and other programming languages and evaluation boards for project development.

Features

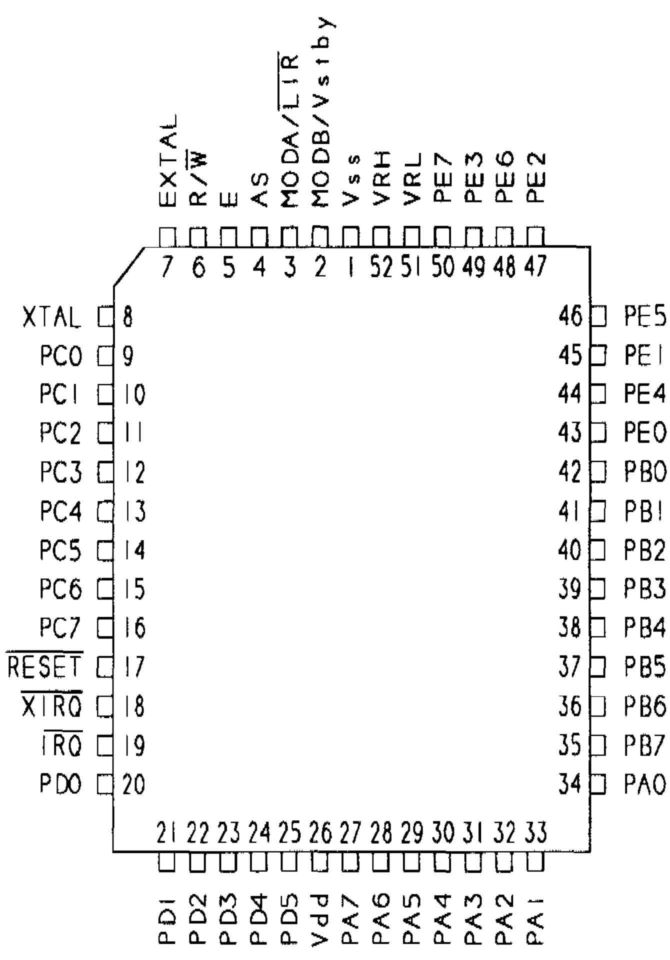
Up to 32K of ROM
Up to 1.2K bytes of RAM
Up to 640 bytes of EEPROM
SPI (Synchronous Serial Peripheral Interface)
SCI (Ansynchronous Serial Communications Interface)
2-MHz bus speed (4-MHz available)
64 eight-bit registers
110 instructions, six address modes
One 16-bit timer, watchdog timer
18 interrupt sources
Eight-channel, eight-bit A/D converter
Up to 62 bits of I/O

Family Members

68HC11A8	8K of ROM, 256 bytes of RAM, 512 bytes of EEPROM, eight-bit A/D, 38 bits of I/O
68HC11A1	No of ROM, 256 bytes of RAM, 512 bytes of EEPROM, eight-bit A/D, 38 bits of I/O
68HC11D3	4K of ROM, 192 bytes of RAM, 32 bits of I/O
68HC711D3	4K of EPROM, 192 bytes of RAM, 32 bits of I/O
68HC811E2	2K of EEPROM, 256 bytes of RAM, eight-bit A/D, 38 bits of I/O

68HC916X1 and /Y1 have 48K Flash EPROM program memory
Alternate packages include 48-pin DIP (port E is 4 bits)
68HC(7)11D3 uses a 40-pin DIP or 44-lead PLCC

Pin	Function
1	Circuit Ground
2	Mode Select B; Standby voltage
3	ModeSselect A; Load Instruction Register
4	Strobe A Input; Address Strobe Output
5	E Clock Output
6	Strobe B Output; Read/Write Select
7	External Clock Input
8	Crystal Driver
9	Port C, Bit 0; Address/Data Bit 0
10	Port C, Bit 1; Address/Data Bit 1
11	Port C, Bit 2; Address/Data Bit 2
12	Port C, Bit 3; Address/Data Bit 3
13	Port C, Bit 4; Address/Data Bit 4
14	Port C, Bit 5; Address/Data Bit 5
15	Port C, Bit 6; Address/Data Bit 6
16	Port C, Bit 7; Address/Data Bit 7
17	Reset
18	Non-Maskable External Interrupt Request
19	External Interrupt Request
20	Port D, Bit 0; SCI Receive Data Input
21	Port D, Bit 1; SCI Transmit Data Output
22	Port D, Bit 2; SPI Master Input/Slave Output
23	Port D, Bit 3; SPI Master Output/Slave input
24	Port D, Bit 4; SPI Serial Clock
25	Port D, Bit 5; SPI Slave Select
26	Supply Voltage
27	Port A, Bit 7; Input Capture 3
28	Port A, Bit 6; Input Aapture 2
29	Port A, Bit 5; Input Capture 1
30	Port A, Bit 4; Output Compare 5 and/or Output Compare 1
31	Port A, Bit 3; Output Compare 4 and/or Output Compare 1
32	Port A, Bit 2; Output Compare 3 and/or Output Compare 1
33	Port A, Bit 1; Output Compare 2 and/or Output Compare 1
34	Port A, Bit 0; Pulse Accumulator Input and/or Output Compare 1
35	Port B, Bit 7; Address Bit 15
36	Port B, Bit 6; Address Bit 14
37	Port B, Bit 5; Address Bit 13
38	Port B, Bit 4; Address Bit 12
39	Port B, Bit 3; Address Bit 11
40	Port B, Bit 2; Address Bit 10
41	Port B, Bit 1; Address Bit 9
42	Port B, Bit 0; Address Bit 8
43	Port E, Bit 0; Analog Input 0
44	Port E, Bit 4; Analog Input 4
45	Port E, Bit 1; Analog Input 1
46	Port E, Bit 5; Analog Input 5
47	Port E, Bit 2; Analog Input 2
48	Port E, Bit 6; Analog Input 6
49	Port E, Bit 3; Analog Input 3
50	Port E, Bit 7; Analog Nnput 7
51	Low Reference Voltage
52	High Reference Voltage



68HC11
PLCC

Manufacturers (See 68HC05)

Zilog Z8

Summary

The Z8 can address up to 64K bytes each of data and program memory. The only on-chip RAM is a register file that includes I/O, status, control and general-purpose registers. There are four external interrupt pins and optional handshaking signals for the ports. Because a pin may have as many as four alternate functions, not all capabilities are available at once.

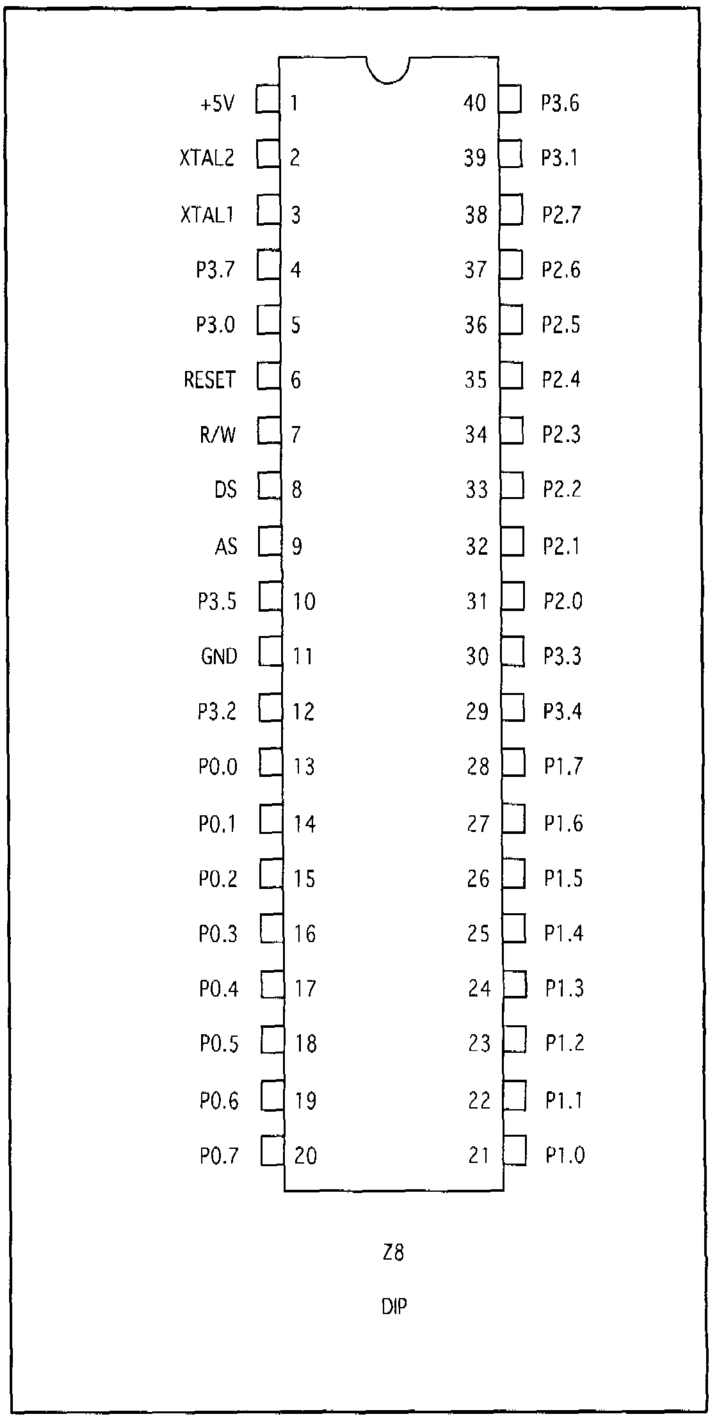
Features

Up to 20K of ROM
12.5-MHz clock (25-MHz available)
144 to 256 eight-bit registers
Serial port
Eight interrupt sources
32 bits of I/O
Two eight-bit timers
43 instructions, six address modes

Family members

Z8601 2K of ROM, 144-byte register file with 32 bits of I/O
Z8611 4K of ROM, 144-byte register file with 32 bits of I/O
Z8600 2K of ROM, 144-byte register file with 22 bits of I/O
Z86C21 8K of ROM, 256-byte register file with 32 bits of I/O, CMOS
Z8671 includes BASIC/Debug in ROM
Z8603 and Z8613 have piggyback EPROM sockets
PLCC package also available

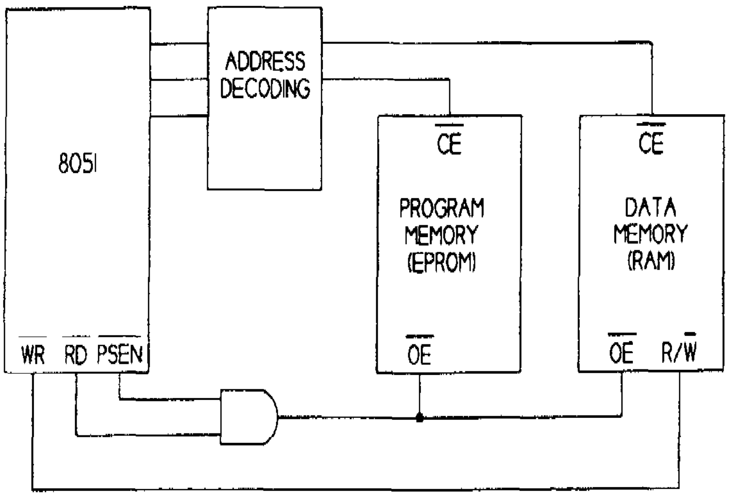
Pin	Function
1	Supply Voltage
2	Crystal 2 (Timebase Output)
3	Crystal 1 (Timebase Input)
4	Port 3, Bit 7; Serial Output
5	Port 3, Bit 0; Serial Input; Interrupt Request 3
6	Reset
7	Read/Write Select
8	Data Strobe
9	Address Strobe
10	Port 3, Bit 5; Port 0 Ready; Data Available
11	Circuit Ground
12	Port 3, Bit 2; Port 0 Data Available/Ready; Interrupt Request 2
13	Port 0, Bit 0; Address Bit 8
14	Port 0, Bit 1; Address Bit 9
15	Port 0, Bit 2; Address Bit 10
16	Port 0, Bit 3; Address Bit 11
17	Port 0, Bit 4; Address Bit 12
18	Port 0, Bit 5; Address Bit 13
19	Port 0, Bit 6; Address Bit 14
20	Port 0, Bit 7; Address Bit 15
21	Port 1, Bit 0; Address/Data Bit 0
22	Port 1, Bit 1; Address/Data Bit 1
23	Port 1, Bit 2; Address/Data Bit 2
24	Port 1, Bit 3; Address/Data Bit 3
25	Port 1, Bit 4; Address/Data Bit 4
26	Port 1, Bit 5; Address/Data Bit 5
27	Port 1, Bit 6; Address/Data Bit 6
28	Port 1, Bit 7; Address/Data bit 7
29	Port 3, Bit 4; Port 1 Ready/Data Available; Data Memory Select
30	Port 3, Bit 3; Port 1 Data Available/Ready; Interrupt Request 3
31	Port 2, Bit 0
32	Port 2, Bit 1
33	Port 2, Bit 2
34	Port 2, Bit 3
35	Port 2, Bit 4
36	Port 2, Bit 5
37	Port 2, Bit 6
38	Port 2, Bit 7
39	Port 3, Bit 1; Port 2 Data Available/Ready; Interrupt Request 2; Timer Input
40	Port 3, Bit 6; Port 2 Ready/Data Available; Timer Output



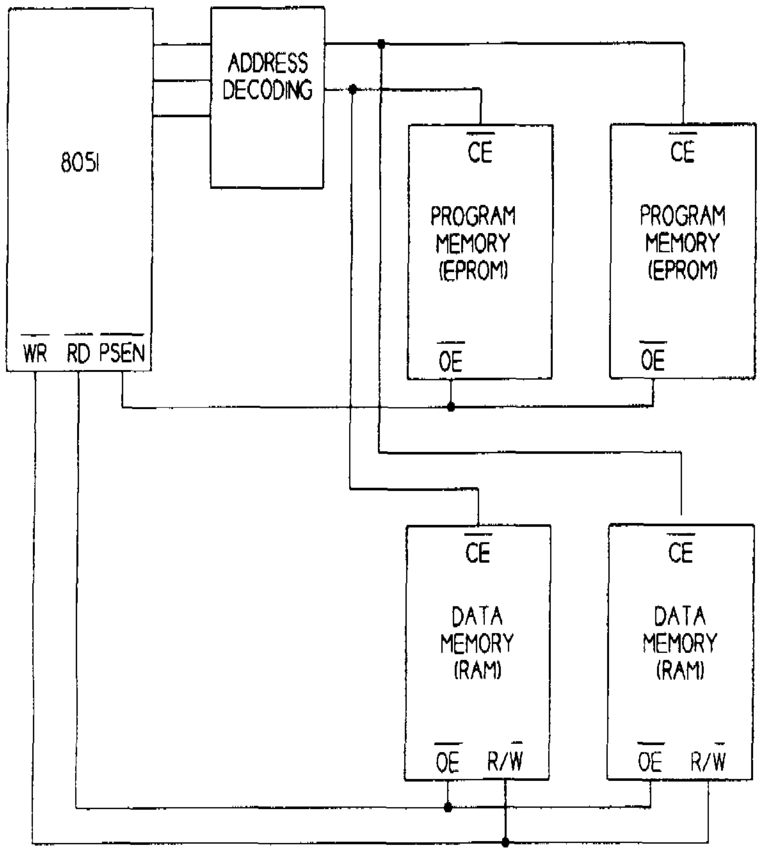
Manufacturer

Zilog, Inc.
210 Hacienda Ave.
Campbell, CA 95008-6609
Tel.: 408-370-8000

Additional Information

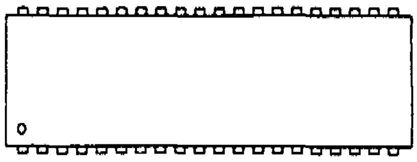


Combined program/data memory area

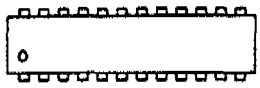


Separate program and data memory areas

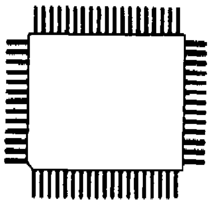
With the 8051 and some other chips, you can double the amount of addressable memory by establishing separate program and data memory areas. Program memory is read with PSEN and cannot be written to. Data memory is accessed with RD and WR.



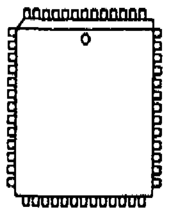
40-pin DIP (dual in-line package)



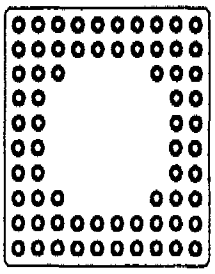
24-pin skinny DIP



64-lead QFP
(quad flat pack)

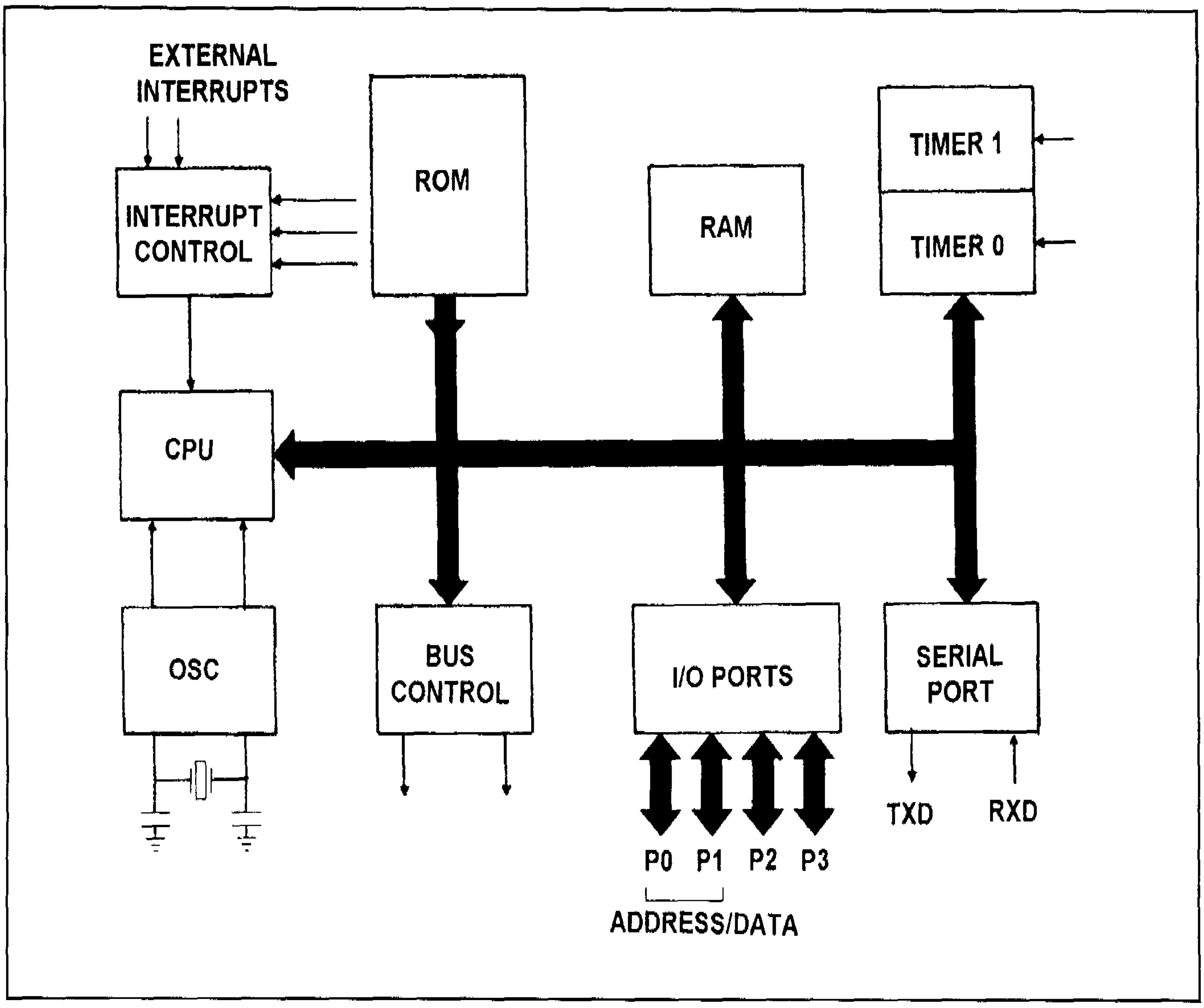


52-lead PLCC
(plastic leaded
chip carrier)



68-pin PGA
(pin grid array)

Examples of popular packages for microcomputer chips.



Block diagram of the 8051 core shared by all 8051 family members.

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ComputerCraft

ComputerCraft Magazine's Guide To EPROMs

EPROMs (Erasable, Programmable, Read-Only Memory) are integrated circuits that permanently store programs, data, or other information, with the option to erase and reprogram when needed. EPROMs are a popular choice for storing programs in embedded controllers and other single-board computers that don't use disk storage. Some personal computers use EPROMs to store BIOS routines.

You can identify an EPROM by its clear window, which allows you to erase the contents by exposing the circuits to ultraviolet energy. After programming, the window should be covered with an opaque label to prevent accidental erasing.

When you don't plan to erase, a low-cost option is the one-time-only PROM, or OTP PROM. An OTP PROM is an EPROM without the window. Many developers use EPROMs during product development and switch to OTP versions when a design is final and ready for production.

EPROMs are available in many capacities. In this tenth installment of our series on special series of pull-out data guides, the focus is on pinouts for popular EPROMs, a review of signal functions and a summary of file formats for EPROM programming.

Prepared by Jan Axelson
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76 North Broadway, Hicksville, NY 11801

24-Pin EPROMs

You can find 24-pin EPROMs in capacities from 2K to 8K. Motorola's 68764 EPROM matches the pinout of the 2364 ROM, which stored BIOS routines and BASIC in the original IBM PC.

28-Pin EPROMs

These 28-pin devices have capacities from 8K to 64K. Although there are 8K EPROMs in 24-pin packages, the 28-pin 2764 is more common. Pinout patterns are similar to the 24-pin pinouts, if you "bottom-justify" the 24-pin device so that its pin 1 aligns with pin 3 of the 28-pin device.

32-Pin EPROMs

For storing 128K to 1M byte, 32-pin EPROMs will do the job. These also follow the pinout pattern used in smaller-capacity devices, with minor differences.

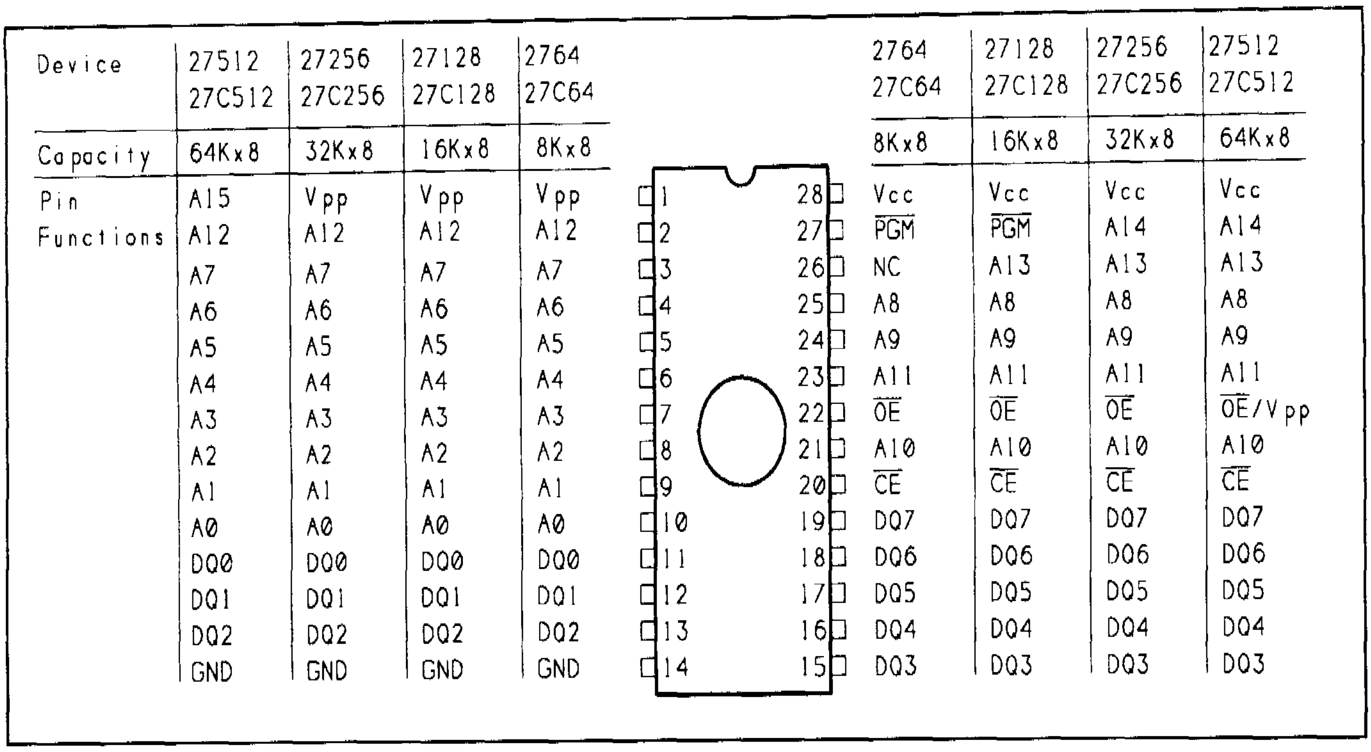
40-Pin EPROMs

These 40-pin EPROMs are word-wide. That is, they store 16 bits at each address, compared to eight bits per address for the preceding devices. For example, the 27C210 stores 64K 16-bit words, or 1M bit.

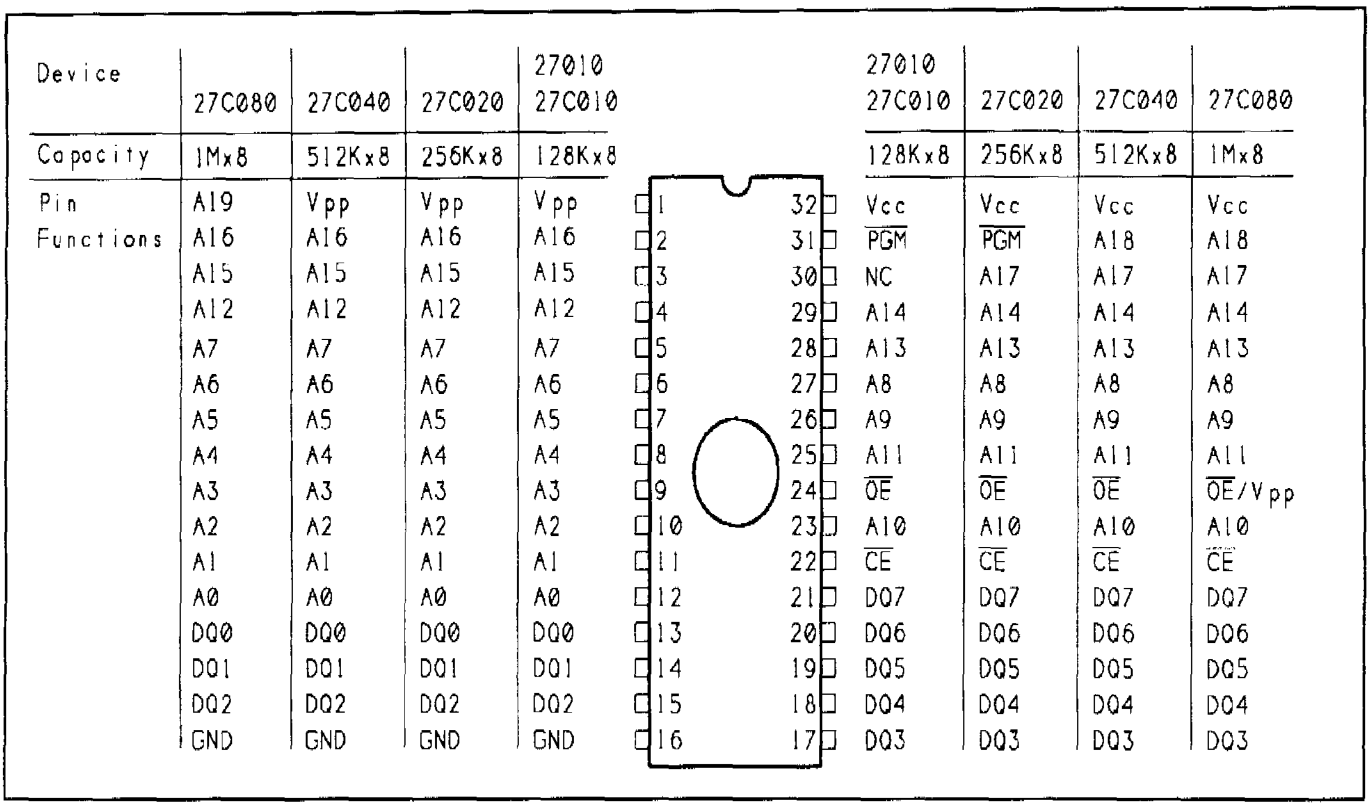
EPROM Pin Functions

Symbol	Type	Function	Comments
A0 thru A19	Input	Address	Number of address inputs indicates how many bytes or words EPROM can store. For example, a 2716 has 11 address inputs (A0 thru A10) and stores 2^{11} (2,048) bytes.
DQ1 thru DQ16	Output	Data	Byte-wide EPROMs have eight data pins (DQ1 thru DQ8); word-wide EPROMs have 16. Sometimes labeled O0 thru O7 (Outputs 0 thru 7). Act as inputs during programming.

Device	68764	2732 27C32	2716			2716	2732 27C32	68764
Capacity	8Kx8	4Kx8	2Kx8			2Kx8	4Kx8	8Kx8
Pin Functions	A7	A7	A7	1	24	Vcc	Vcc	Vcc
	A6	A6	A6	2	23	A8	A8	A8
	A5	A5	A5	3	22	A9	A9	A9
	A4	A4	A4	4	21	Vpp	A11	A12
	A3	A3	A3	5	20	$\overline{\text{OE}}$	$\overline{\text{OE}}$/Vpp	$\overline{\text{E}}$/Vpp
	A2	A2	A2	6	19	A10	A10	A10
	A1	A1	A1	7	18	$\overline{\text{CE}}$	$\overline{\text{CE}}$	A11
	A0	A0	A0	8	17	DQ7	DQ7	DQ7
	DQ0	DQ0	DQ0	9	16	DQ6	DQ6	DQ6
	DQ1	DQ1	DQ1	10	15	DQ5	DQ5	DQ5
	DQ2	DQ2	DQ2	11	14	DQ4	DQ4	DQ4
	GND	GND	GND	12	13	DQ3	DQ3	DQ3



Device	27512 27C512	27256 27C256	27128 27C128	2764 27C64			2764 27C64	27128 27C128	27256 27C256	27512 27C512
Capacity	64Kx8	32Kx8	16Kx8	8Kx8			8Kx8	16Kx8	32Kx8	64Kx8
Pin Functions	A15	Vpp	Vpp	Vpp	1	28	Vcc	Vcc	Vcc	Vcc
	A12	A12	A12	A12	2	27	$\overline{PGM}$	$\overline{PGM}$	A14	A14
	A7	A7	A7	A7	3	26	NC	A13	A13	A13
	A6	A6	A6	A6	4	25	A8	A8	A8	A8
	A5	A5	A5	A5	5	24	A9	A9	A9	A9
	A4	A4	A4	A4	6	23	A11	A11	A11	A11
	A3	A3	A3	A3	7	22	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/Vpp
	A2	A2	A2	A2	8	21	A10	A10	A10	A10
	A1	A1	A1	A1	9	20	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
	A0	A0	A0	A0	10	19	DQ7	DQ7	DQ7	DQ7
	DQ0	DQ0	DQ0	DQ0	11	18	DQ6	DQ6	DQ6	DQ6
	DQ1	DQ1	DQ1	DQ1	12	17	DQ5	DQ5	DQ5	DQ5
	DQ2	DQ2	DQ2	DQ2	13	16	DQ4	DQ4	DQ4	DQ4
	GND	GND	GND	GND	14	15	DQ3	DQ3	DQ3	DQ3



Device	27C080	27C040	27C020	27010 27C010			27010 27C010	27C020	27C040	27C080
Capacity	1Mx8	512Kx8	256Kx8	128Kx8			128Kx8	256Kx8	512Kx8	1Mx8
Pin Functions	A19	Vpp	Vpp	Vpp	1	32	Vcc	Vcc	Vcc	Vcc
	A16	A16	A16	A16	2	31	$\overline{PGM}$	$\overline{PGM}$	A18	A18
	A15	A15	A15	A15	3	30	NC	A17	A17	A17
	A12	A12	A12	A12	4	29	A14	A14	A14	A14
	A7	A7	A7	A7	5	28	A13	A13	A13	A13
	A6	A6	A6	A6	6	27	A8	A8	A8	A8
	A5	A5	A5	A5	7	26	A9	A9	A9	A9
	A4	A4	A4	A4	8	25	A11	A11	A11	A11
	A3	A3	A3	A3	9	24	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/Vpp
	A2	A2	A2	A2	10	23	A10	A10	A10	A10
	A1	A1	A1	A1	11	22	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
	A0	A0	A0	A0	12	21	DQ7	DQ7	DQ7	DQ7
	DQ0	DQ0	DQ0	DQ0	13	20	DQ6	DQ6	DQ6	DQ6
	DQ1	DQ1	DQ1	DQ1	14	19	DQ5	DQ5	DQ5	DQ5
	DQ2	DQ2	DQ2	DQ2	15	18	DQ4	DQ4	DQ4	DQ4
	GND	GND	GND	GND	16	17	DQ3	DQ3	DQ3	DQ3

Symbol	Type	Function	Comments
-CE	Input	Chip Enable	Power control and device select. Must be low to read data. Sometimes called CS (chip select) or E (enable).
GND	Input	Circuit Ground	
NC	—	No Connection	
-OE	Input	Output Enable	Gates data to outputs. Must be low to read data. Also called G.
-PGM	Input	Program Enable	Pulses low during programming. EPROMs without PGM pin pulse CE instead.
V_{cc}	Input	Power Supply	+5 volts. Sometimes raised to 6 or 6.25 volts during programming.
V_{PP}	Input	Programming Supply	Applied only during programming. Voltage varies from 12.5 to 25 volts, depending on the chip and program ming algorithm. Sometimes shares the same pin with OE.

File Formats for EPROM Programming

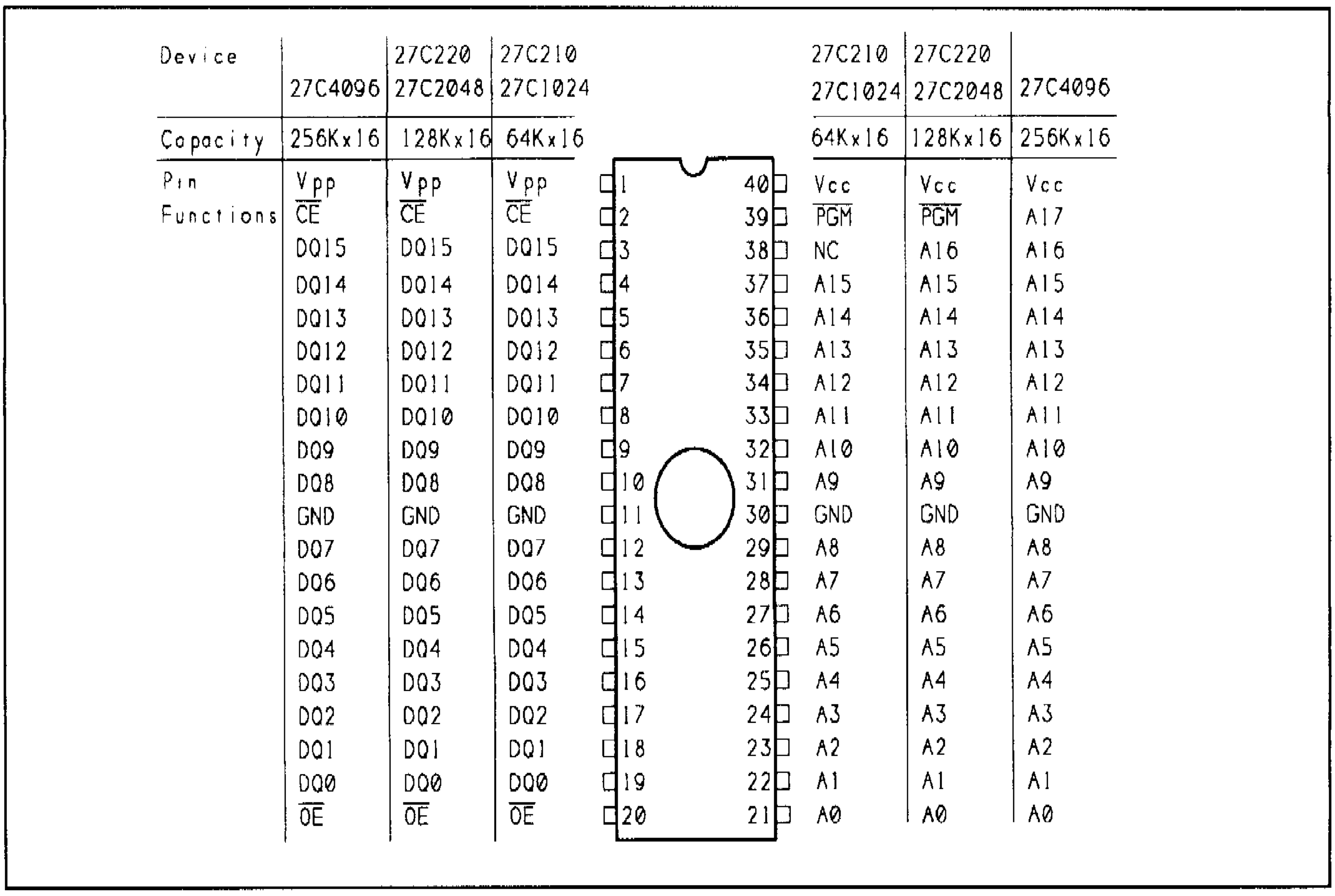
Most EPROM programmers are able to program EPROMs directly from files created by assemblers and compilers, but the file must be in a format that the programmer recognizes. Four common formats are binary, ASCII Hex, Intel Hex and Motorola S-Record.

Binary Format

A binary file consists of a sequence of bytes that exactly corresponds to the bytes to be programmed. The file contains no addressing information for loading or programming and no error-checking. To view or edit a binary file, you need a special file-viewing utility. Conventional file-viewing techniques, such as DOS's TYPE command, display the bytes as ASCII characters. For example, the value "1" appears on-screen as a happy-face character. Binary format is sometimes called executable format.

ASCII Hex Format

In ASCII Hex, or "pure" Hex, format, each byte is expressed as a two-character hexadecimal number, with each character stored as its ASCII code. ASCII Hex files contain only these 16 codes: 30h through 39h



Device	27C4096	27C220 27C2048	27C210 27C1024			27C210 27C1024	27C220 27C2048	27C4096
Capacity	256Kx16	128Kx16	64Kx16			64Kx16	128Kx16	256Kx16
Pin Functions	Vpp	Vpp	Vpp	1	40	Vcc	Vcc	Vcc
	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	2	39	$\overline{PGM}$	$\overline{PGM}$	A17
	DQ15	DQ15	DQ15	3	38	NC	A16	A16
	DQ14	DQ14	DQ14	4	37	A15	A15	A15
	DQ13	DQ13	DQ13	5	36	A14	A14	A14
	DQ12	DQ12	DQ12	6	35	A13	A13	A13
	DQ11	DQ11	DQ11	7	34	A12	A12	A12
	DQ10	DQ10	DQ10	8	33	A11	A11	A11
	DQ9	DQ9	DQ9	9	32	A10	A10	A10
	DQ8	DQ8	DQ8	10	31	A9	A9	A9
	GND	GND	GND	11	30	GND	GND	GND
	DQ7	DQ7	DQ7	12	29	A8	A8	A8
	DQ6	DQ6	DQ6	13	28	A7	A7	A7
	DQ5	DQ5	DQ5	14	27	A6	A6	A6
	DQ4	DQ4	DQ4	15	26	A5	A5	A5
	DQ3	DQ3	DQ3	16	25	A4	A4	A4
	DQ2	DQ2	DQ2	17	24	A3	A3	A3
	DQ1	DQ1	DQ1	18	23	A2	A2	A2
	DQ0	DQ0	DQ0	19	22	A1	A1	A1
	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	20	21	A0	A0	A0

(for the numerals 0 through 9) and 41h through 46h (for the letters A through F).

You can view and edit ASCII Hex files on-screen, because the computer displays the codes as the ASCII characters they represent. The EPROM programmer must translate the codes into binary data for programming. Because each byte to be programmed requires two codes, an ASCII Hex file is twice as long as the resulting file programmed into the EPROM.

Example translation into ASCII Hex:

Binary Byte	1100	0101
Hex Equivalent	C	5
ASCII Codes (Hex)	43	35

Intel Hex Format

Like ASCII Hex, Intel Hex format stores bytes as ASCII codes that represent hexadecimal characters. Intel Hex also includes addressing and error-checking information for more-flexible programming and more-reliable file transmission.

An Intel Hex file consists of a series of records. Each record ends in a carriage return/line feed (CRLF). Each record contains the following elements, in order:

Name	Characters	Description
Record Mark	1	Each record begins with a colon (:).
Record Length	2	Number of data bytes in the record.
Address Field	2	In data records, address where first data byte is to be stored, with following bytes stored in sequence. In other record types, 0000.
Record Type	2	There are four record types: 00 = Data 01 = End of File 02 = Extended Address 03 = Start Address.
Data Field	Varies	Contents of data field depends on record type: 00 = Data to be Programmed 01 = Not Used (Empty) 02 = Segment (for address fields larger than 64K, data is stored beginning at (segment*10h)+address field For example, an extended address of F800h and an address field of 1000h results in data storage beginning at F9000h. The segment remains valid until a new one is specified. Start address of program. Often unused.
Checksum	2	To calculate the checksum: (1) Add values of all of bytes in a record. (2) Take the 2's complement of the result. (In binary, change 1s to 0s, change 0s to 1s and then add 1.) (3) The checksum is the low byte of the result. If you add the values of all of bytes in a record, including checksum, result should end in 00h.

Example Intel Hex File:

```
:03800000028200F9
:03801300028223C3
:20820000D28AE589440A541FF589D2AF757F00757E00757D00D2
8ED2AAE57FB403FBC2AA9D
:16822000020000C28E858D7D858B7E758D00758B00D28E057F32C1
:00000001FF
```

Example Checksum calculation for line 1:

(1) Sum values of first seven bytes: 107 (Hex), or 100000111 (binary).
(2) Take 2's complement of sum: 011111000 + 1 = 011111001 (binary), or F9 (Hex)
(3) Checksum is F9, final byte in the line.

Motorola S-Record Format

Like Intel Hex, Motorola S-records store bytes as ASCII codes, with added addressing and error-checking. A file in S-record format consists of a series of records. Each record ends in a carriage return/line feed (CRLF). A file with 16-bit addressing often has the extension S19, which describes the two record types it contains.

Each record contains the following elements, in order:

Name	Characters	Description
Record Marker	1	Each record begins with the character "S."
Record Type	1	There are six record types: (1) 16-bit addressing (2) 24-bit addressing (3) 32-bit addressing (7) end of file (32-bit addressing) (8) end of file (16-bit addressing) (9) end of file (32-bit addressing)
Load Address	4,6 or 8	Starting address where data is to be stored.
File Data	Varies	Data to be stored. Not used in end-of-file records.
Checksum	2	To calculate checksum: (1) Add values of all of bytes in a record, except record marker and record type. (2) Take the 1's complement of result. (In binary, change binary 1s to 0s and 0s to 1s.) (3) Checksum is low byte of result. If you add the values of all of the bytes in the record, including the checksum, the result should end in FFh.

Example file in S-record format:

```
S1130200A680B700A6F0B70400000DB600A880B71A
S10F0210005F4F5A26FC20F01E0020EC7A
S10B03F80200020002000200F1
S9030000FC
```

Example checksum calculation for line 3:

(1) Sum values of first 11 bytes: 10E (Hex), or 100001110 (binary).
(2) Take the 1's complement of sum: 011110001 (binary), or F1 (Hex).
(3) Checksum is F1, the final byte in line.

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Corrections

March 1993 Disk Drive Interfaces section transpose the two cable drawings on the first page with those on the second page.

The 80x86 Microprocessor Family
Part 3: The 80486 and Pentium

This is the ninth in our series of special-bonus pull-outs. This time around, we continue our tour of the 80x86 microprocessor family, with a guide to 80486 chips and a look at Intel's new Pentium microprocessor and supply a chart that compares the features of all major members of the 80x86 family.

Prepared By Jan Axelson. Copyright 1993 CQ Communications, Inc.
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80486DX/SX

Summary

The 80486DX enhances the 80386's architecture by adding an on-chip math coprocessor and an 8K memory cache that speeds operation by reducing external memory accesses. The lower-cost 80486SX has no math coprocessor.

Features

- 80386-compatible core
- Up to 50-MHz clock (66 MHz with clock doubler)
- On-chip floating-point unit (math coprocessor; DX only)
- 8-K-byte code and data cache
- Reduced instruction-cycle times
- Burst-transfer mode for fast memory access
- Built-in self-test and debugging aids
- Support for boundary scan test (IEEE Std. 1149.1)
- Physical address space: 4G bytes
- 168-pin PGA package; SX also available in 196-lead PQFP
- Low-power CMOS technology

Related Chips:

Intel's 80486DX was the original '486 chip, followed by the lower-cost 80486SX. The 80486DX2 has a clock doubler that doubles the speed of internal operations. All have 32-bit data paths. Low-power versions are also available.

Cyrix has released a variety of '486 chips. Its Cx486DLC uses a 132-pin PGA package, with a '486SX-compatible instruction set, 1K-byte cache and no math coprocessor. The Cx486SLC is similar but is housed in a 100-lead PLCC with a 16-bit external data bus. The Cx486SLC/E adds power management. The Cx486DRu^2 is a '486 direct replacement upgrade for '386DX's.

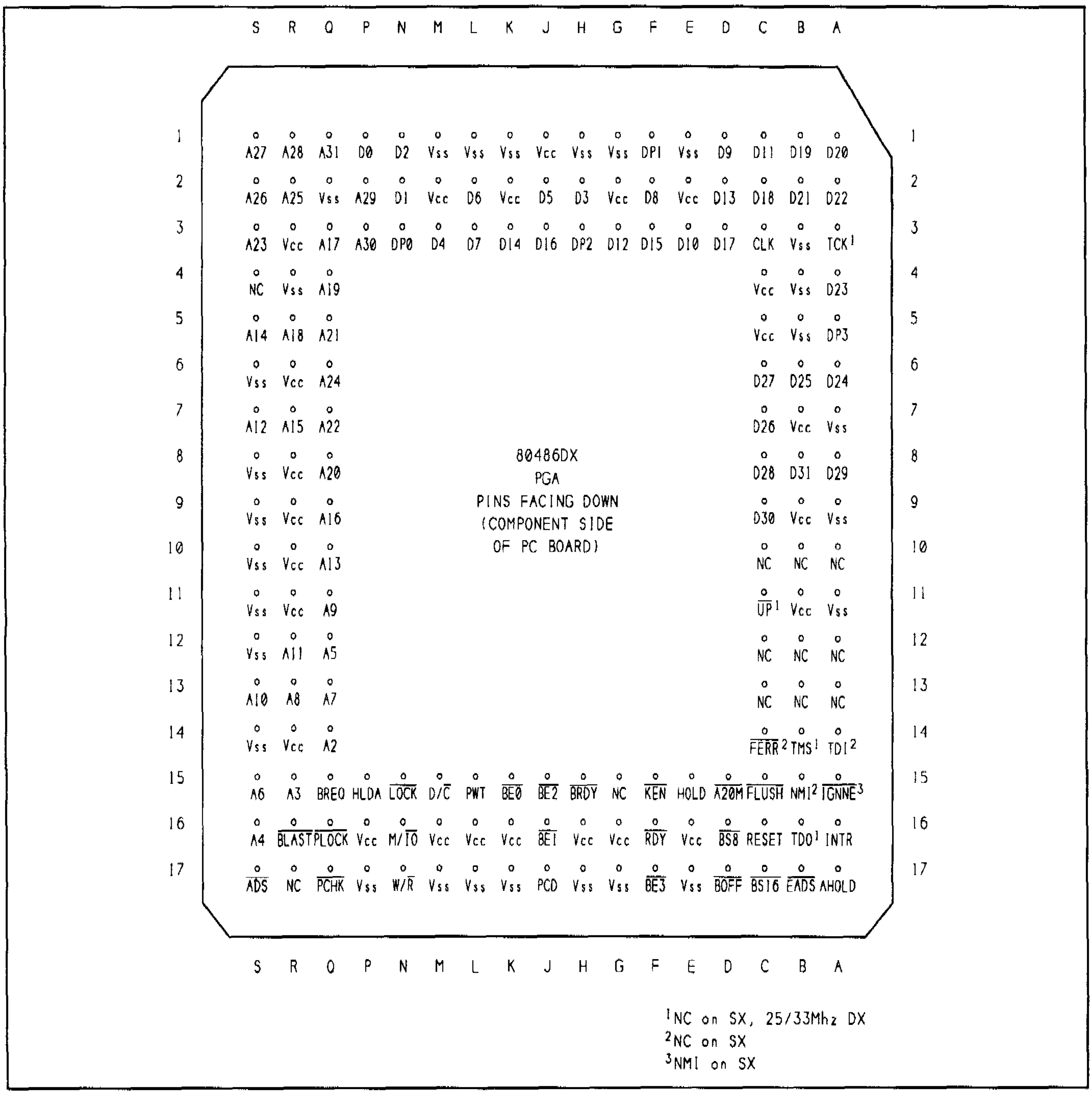
AMD has '486's at 33 and 40 MHz, and at 50 MHz with clock-doubling.

IBM's 486SLC has power management and a 16-bit external data bus and operates at 5 or 3.3 volts.

80486 Pin Reference

Address	Location	
	PGA	PQFP (SX Only)
A2	Q14	146
A3	R15	150
A4	S16	152
A5	Q12	154
A6	S15	158
A7	Q13	159
A8	R13	161
A9	Q11	163
A10	S13	165
A11	R12	172
A12	S7	174
A13	Q10	176
A14	S5	178
A15	R7	180
A16	Q9	181
A17	Q3	183
A18	R5	189
A19	Q4	191
A20	Q8	193
A21	Q5	2
A22	Q7	3
A23	S3	4
A24	Q6	5
A25	R2	7
A26	S2	8
A27	S1	9
A28	R1	10
A29	P2	12
A30	P3	13
A31	Q1	14

Data	Location	
	PGA	PQFP (SX Only)
D0	P1	17
D1	N2	18
D2	N1	20
D3	H2	23
D4	M3	25
D5	J2	26
D6	L2	27
D7	L3	29
D8	F2	31
D9	D1	32
D10	E3	35
D11	C1	37
D12	G3	38
D13	D2	39
D14	K3	41
D15	F3	42
D16	J3	44
D17	D3	45
D18	C2	46
D19	B1	47
D20	A1	48
D21	B2	51
D22	A2	53



	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	A27	A28	A31	D0	D2	Vss	Vss	Vss	Vcc	Vss	Vss	DP1	Vss	D9	D11	D19	D20	1
2	A26	A25	Vss	A29	D1	Vcc	D6	Vcc	D5	D3	Vcc	D8	Vcc	D13	D18	D21	D22	2
3	A23	Vcc	A17	A30	DP0	D4	D7	D14	D16	DP2	D12	D15	D10	D17	CLK	Vss	TCK[1]	3
4	NC	Vss	A19												Vcc	Vss	D23	4
5	A14	A18	A21												Vcc	Vss	DP3	5
6	Vss	Vcc	A24												D27	D25	D24	6
7	A12	A15	A22												D26	Vcc	Vss	7
8	Vss	Vcc	A20												D28	D31	D29	8
9	Vss	Vcc	A16												D30	Vcc	Vss	9
10	Vss	Vcc	A13												NC	NC	NC	10
11	Vss	Vcc	A9												$\overline{\text{UP}}$[1]	Vcc	Vss	11
12	Vss	A11	A5												NC	NC	NC	12
13	A10	A8	A7												NC	NC	NC	13
14	Vss	Vcc	A2												$\overline{\text{FERR}}$[2]	TMS[1]	TDI[2]	14
15	A6	A3	BREQ	HLDA	$\overline{\text{LOCK}}$	D/$\overline{\text{C}}$	PWT	$\overline{\text{BE0}}$	$\overline{\text{BE2}}$	$\overline{\text{BRDY}}$	NC	$\overline{\text{KEN}}$	HOLD	$\overline{\text{A20M}}$	$\overline{\text{FLUSH}}$	NMI[2]	$\overline{\text{IGNNE}}$[3]	15
16	A4	$\overline{\text{BLAST}}$	$\overline{\text{PLOCK}}$	Vcc	M/$\overline{\text{IO}}$	Vcc	Vcc	Vcc	$\overline{\text{BE1}}$	Vcc	Vcc	$\overline{\text{RDY}}$	Vcc	$\overline{\text{BS8}}$	RESET	TDO[1]	INTR	16
17	$\overline{\text{ADS}}$	NC	$\overline{\text{PCHK}}$	Vss	W/$\overline{\text{R}}$	Vss	Vss	Vss	PCD	Vss	Vss	$\overline{\text{BE3}}$	Vss	$\overline{\text{BOFF}}$	$\overline{\text{BS16}}$	$\overline{\text{EADS}}$	AHOLD	17
	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

80486DX
PGA
PINS FACING DOWN
(COMPONENT SIDE
OF PC BOARD)

[1] NC on SX, 25/33Mhz DX
[2] NC on SX
[3] NMI on SX

D23	A4	55
D24	A6	59
D25	B6	61
D26	C7	63
D27	C6	65
D28	C8	67
D29	A8	69
D30	C9	71
D31	B8	74

Control	**Location**	
	PGA	**PQFP (SX Only)**
-A20M	D15	104
-ADS	S17	145
AHOLD	A17	129
-BE0	K15	117
-BE1	J16	116
-BE2	J15	115
-BE3	F17	113
-BLAST	R16	144
-BOFF	D17	137
-BRDY	H15	138
-BREQ	Q15	118
-BS8	D16	135
-BS16	C17	136
CLK	C3	123
D/-C	M15	110
DP0	N3	16
DP1	F1	30
DP2	H3	43
DP3	A5	57
-EADS	B17	105
-FERR	C14 (DX, DX2 Only)	—
-FLUSH	C15	102
HLDA	P15	122
HOLD	E15	130
-IGNNE	A15 (DX, DX2 Only)	—
-INTR	A16	101
-KEN	F15	132
-LOCK	N15	142
M/-IO	N16	111
NMI	A15 (SX Only)	100
NMI	B15 (DX, DX2 Only)	—
-PCD	J17	106
-PCHK	Q17	139
PWT	L15	108
-PLOCK	Q16	143
-RDY	F16	133
RESET	C16	103
-UP	(DX2, 50-MHz DX Only)	—
-W/-R	N17	120

Note: Leading hyphen means a signal is active low

Test	**Location**	
	PGA	**PQFP (SX Only)**
TCK	A3 (DX2, 50-MHz DX Only)	128

TDI	A14 (DX2, 50-MHz DX Only)	185
TDO	B16 (DX2, 50-MHz DX Only)	80
TMS	B14 (DX2, 50-MHz DX Only)	187

No Connection	Location	
	PGA	PQFP (SX Only)
N.C.	A3 (SX, 25/33-MHz DX Only)	15
	A10	34
	A12	52,56
	A13	60,64,68
	A14 (SX, 25/33-MHz DX Only)	72,73,75 thru 79
	B12	81-83,85,87 thru 89
	B13	90-92,94,97
	B14 (SX, 25/33-MHz DX Only)	124,127
	B15 (SX Only)	134
	B16 (SX, 25/33-MHz DX Only)	140,149
	C10	151,153,155,157
	C13	160,162,166,169
	C14 (SX Only) 171,173	
	G15	186,188
	R17	190,192,195
	S4	

Power	Location	
	PGA	PQFP (SX only)
V_{cc}	B7	6
	B9	19
	B11	24
	C4	28
	C5	36
	E2	49
	E16	54
	G2	62
	G16	70
	H16	84
	J1	93
	K2	98
	K16	107
	L16	112
	M2	119
	M16	125
	P16	131
	R3	147
	R6	164
	R8	170
	R9	175
	R10	179
	R11	184
	R14	196
V_{ss} (GND)		
	A7	1
	A9	11
	A11	21
	B3	22
	B4	33
	B5	40
	E1	50
	E17	58
	G1	66
	G17	86
	H1	95
	H17	96
	K1	99
	K17	109
	L1	114
	L17	121
	M1	126
	M17	141
	P17	148
	Q2	167
	R4	168
	S6	177
	S8	182
	S9	194
	S10	
	S11	
	S12	
	S14	

80486 Pin Descriptions

Symbol	Type	Function
A4 Thru A31	I/O	Address Bus, Address Inputs for Cache-Line Invalidation
A2-A3	Output	Address Bus
-A20M	Input	Address Bit 20 Mask for 8086 Emulation
-ADS	Output	Address Status (First Clock of Bus Cycle)
AHOLD	Input	Address Hold for Cache-Invalidation Cycle
-BE0 Thru BE3	Output	Data Byte Enable (0 Thru 3)
-BLAST	Output	Last Burst Cycle
-BOFF	Input	Back Off (Bus Float)
-BRDY	Input	Burst Ready (Bus Cycle Complete)
BREQ	Output	Bus Request
-BS16	Input	Data Bus Size 16
-BS8	Input	Data Bus Size 8
CLK	Input	System Clock
D0 Thru D31	I/O	Data Bus
D/-C	Output	Bus Data/Control Select
DP0 Thru DP3	I/O	Data Parity (0-3)
-EADS	Input	External Address Strobe for Cache-Invalidation Cycle
-FERR	Output	Floating-Point Error (DX, DX2 Only)
-FLUSH	Input	Flush Internal Cache
HOLDA	Output	Bus Hold Acknowledge
HOLD	Input	Bus Hold Request
-IGNNE	Input	Ignore Numeric Error (DX, DX2 Only)
INTR	Input	Interrupt Request
-KEN	Input	Cache Enable
-LOCK	Output	Bus Lock
M/-IO	Output	Memory or I/O Select
N.C.	—	No Connection
NMI	Input	Nonmaskable-Interrupt Request
PCD	Output	Page Cache Disable
-PCHK	Output	Parity Status Check
-PLOCK	Output	Pseudo Bus Lock for Long Reads and Writes
PWT	Output	Page Write-Through
-RDY	Input	Non-Burst Bus Ready (Bus Cycle Complete)
RESET	Input	System Reset
TCK	Input	Test Clock (Not Present on 25- and 33-MHz DXs)
TDI	Input	Serial Test Data Input (Not Present on 25- and 33-MHz DXs)
TDO	Output	Serial Test Data Output (Not Present on 25- and 33-MHz DXs)
TMS	Input	Test Mode Select (Not Present on 25- and 33-MHz DXs)
-UP	Input	Upgrade Processor Present (DX2 Only)
Vcc	Input	System Power (+5 Volts)
Vss	Input	System Ground
W/-R	Output	Bus Write/Read Select

Note: Leading hyphen means a signal is active low

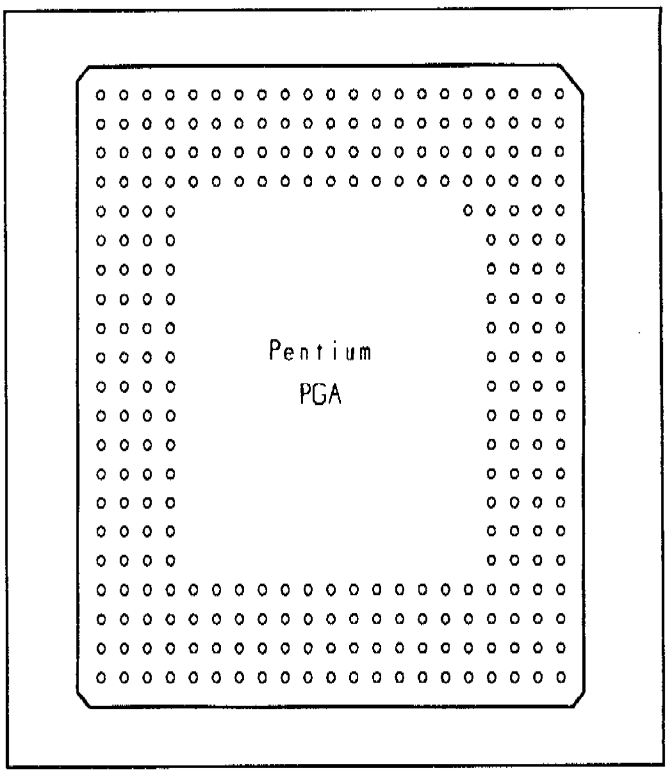
Pentium

Summary

The latest development in 80x86 chips is the Intel Pentium, which has faster performance, a 64-bit external data bus and expanded test and debugging features. Its superscalar architecture has a dual pipeline that can execute multiple instructions simultaneously. The chip is manufactured with a BiCMOS process technology that combines bipolar transistors for speed and CMOS technology for low power and high density.

Features

Code-compatible with 80x86 chips, with improved performance
60- and 66-MHz clock
64-bit external data bus, 32-bit internal
Physical address space: 4G bytes
Separate 8K-byte code and data caches
Superscalar architecture for increased speed
Branch prediction anticipates and pre-loads instructions
Enhanced floating-point unit (math coprocessor)
Reduced instruction-cycle times
Expanded test and debugging aids
273-pin PGA package
BiCMOS technology



Manufacturer Addresses

For more information about the 80x86 chips described in this series, contact the manufacturers listed below:

AMD (Advanced Micro Devices)
901 Thompson Pl.
Sunnyvale, CA 94088
Tel.: 408-732-2400; 1-800-222-9323 (Literature)

Chips & Technologies
3050 Zanker Rd.
San Jose, CA 95134
Tel.: 408-434-0600

Cyrix Corp.
2703 N. Central Expwy.
Richardson, TX 75080
Tel.: 214-234-8387

Fujitsu Microelectronics
Integrated Circuits Div.
3545 N. First St.
San Jose, CA 95134
Tel.: 408-922-9000

Harris Semiconductor
P.O. Box 883
Melbourne, FL 32901
Tel.: 407-724-7800

Intel Literature
(Currently the only source of information on the Pentium)
P.O. Box 7641
Mt. Prospect, IL 60056-7641
1-800-548-4725
Tel.: 408-765-1596

NEC Electronics
401 Ellis St.
P.O. Box 7241
Mountain View, CA 94039
415-960-6000
Tel.: 1-800-632-3531 (Literature)

Siemens Components
2191 Laurelwood Rd.
Santa Clara, CA 95054
Tel.: 408-980-4500

Feature Summary of 80x86 Microprocessors

Chip	Data Path, Internal (Bits)	Data Path, External (Bits)	Address Bus (Bits)	Clock Speed (MHz)	On-Chip Coprocessor	On-Chip Cache (Bytes)	Power Supply (Volts)	Package	Process	Comments
8088	16	8	20	10	No	No	+5	DIP	NMOS, CMOS	Low System Cost
8086	16	16	20	10	No	No	+5	DIP	NMOS, CMOS	Original Chip
80188	16	8	20	10	No	No	+5	LCC,PGA, PLCC	NMOS, CMOS	On-Chip Peripherals
80186	16	16	20	10	No	No	+5	LCC,PGA, PLCC	NMOS, CMOS	On-Chip Peripherals
80286	16	16	24	25	No	No	+5	LCC,PGA, PLCC	NMOS, CMOS	Fast 8086
80386SX	32	16	24	40	No	No	+5,+3.3	PQFP	CMOS	Low-Cost '386
80386DX	32	32	32	40	No	No	+5,+3.3	PGA	CMOS	Improved Memory Management
80486SX	32	32	32	40	No	8	+5,+3.3	PGA,PQFP	CMOS	Low-Cost '486
80486DX	32	32	32	40	Yes	8	+5	PGA,PQFP	CMOS	Burst Transfer Mode
80486DX2	32	32	32	33 Ext. 66 Int.	Yes	8	+5	PGA	CMOS	Clock Doubler
Pentium	32	64	32	66	Yes	Two 8K	+5	PGA	BiCMOS	Superscalar Architecture

ComputerCraft Magazine's PC & Microcontroller Data Guide

In this seventh installment of our continuing series of pull-out data guides for PCs and microcontrollers, Our focus here is on the 80x86 family of microprocessors are the brains inside the millions of personal computers described as "IBM-compatible." From the original 8086, the family has grown to include chips that are faster, use less power or have other added features or/and improvements. This month's quick-reference guide introduces the 8086/8 and 80186/8.

Prepared by Jan Axelson. Copyright 1993 CQ Communications, Inc.
76 North Broadway, Hicksville, NY 11801

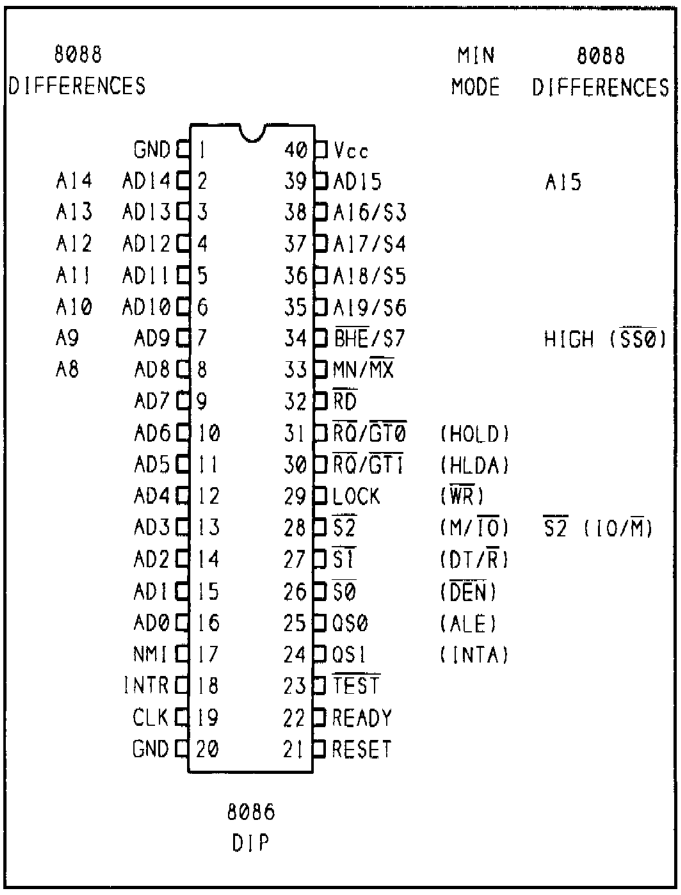
Intel 8086/8

Summary

The 8086 was Intel's first microprocessor with a 16-bit internal and external data bus, which gave it faster performance than existing eight-bit microprocessors. The 8088 is nearly identical, but it has an eight-bit external data bus. You can find 8088s inside original IBM PCs and XTs and many compatibles. Some modern hand-held computers also use 8086/8 chips.

Features

- Up to 10-MHz clock
- Eight and 16-bit signed and unsigned arithmetic
- Binary and decimal operations
- Multiply and divide instructions
- 89 instructions
- 1M addressing ability
- Minimum mode for small embedded systems
- Maximum mode for PCs and multiprocessor systems



Signal	Pin(s)	Type	Function*
AD0-AD7	9-16	I/O	Low Address/Data Bus
AD8-AD15	2-8,39	I/O	High Address/Data Bus (8086 Only)
A8-A15	2-8,39	Output	High Address Bus (8088 Only)
A16/S3	38	Output	Address/Status 3
A17/S4	37	Output	Address/Status 4
A18/S5	36	Output	Address/Status 5
A19/S6	35	Output	Address/Status 6
-BHE/S7	34	Output	Bus High Enable/Status 7 (8086 Only)
CLK	19	Input	Clock
GND	1,20	Input	Ground
HIGH/-SS0	34	Output	High/Status Line (8088 Only)
INTR	18	Input	Interrupt Request
LOCK (-WR)	29	Output	Bus Lock (Write Memory or I/O)
MN/-MX	33	Input	Minimum/Maximum Mode Select
NMI	17	Input	Nonmaskable Interrupt Request
QS0 (ALE)	25	Output	Queue Status 0 (Address Latch Enable)
QS1 (INTA)	24	Output	Queue Status 1 (Interrupt Acknowledge)
RESET	21	Input	System Reset
-RD	32	Output	Read Memory or I/O
READY	22	Input	Ready Acknowledge
-RQ/-GT0 (HOLD)	31	I/O	Bus Request/Grant 0 (Hold)
-RQ/-GT1 (HLDA)	30	I/O	Bus Request/Grant 1 (Hold Acknowledge)

S0 (-DEN)	26	Output	Status 0 (Data Enable)
S1 (DT/-R)	27	Output	Status 1 (Data Transmit/Receive)
S2 (M/-IO)	28	Output	Status 2 (Memory or I/O Select) (8086 Only)
S2 (IO/-M)	28	Output	Status 2 (I/O or Memory Select) (8088 Only)
-TEST	23	Input	Wait Instruction Continues if Low
Vcc	40	Input	Power Supply (+5V)

*Minimum-mode functions are in parentheses.

Related chips

CMOS versions are available (80C86/8).
The NEC V20 and V30 are drop-in replacements for the 8088 and 8086, respectively, that faster performance.
Chips & Technologies' F8680 is an entire PC/XT motherboard on a chip.

Intel 80186/8

Summary

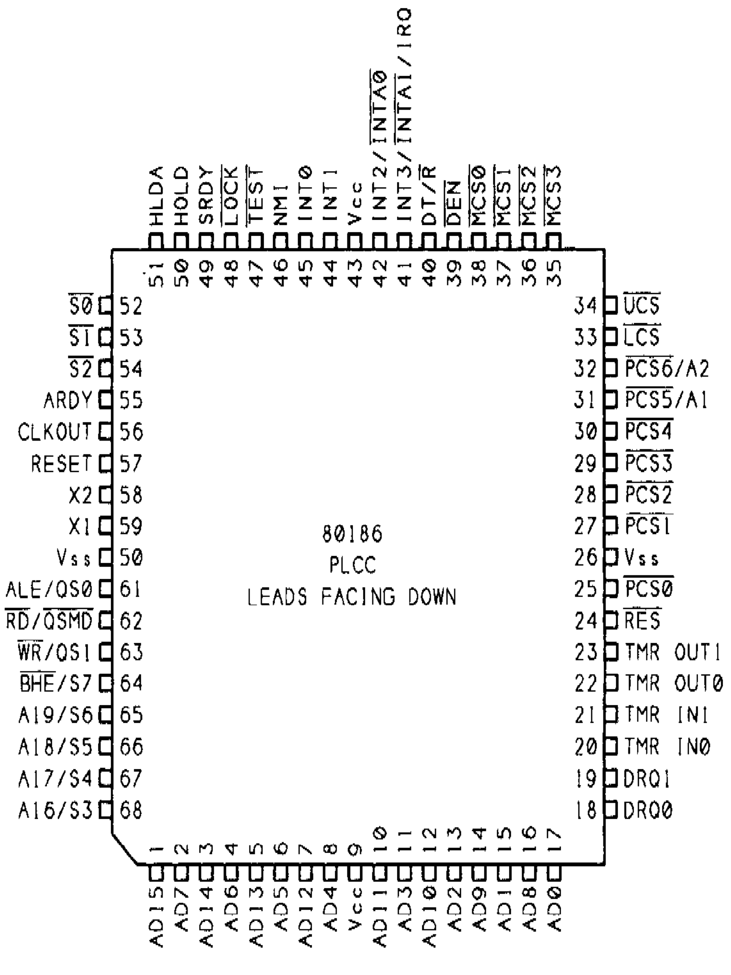
The 80186 contains an 8086 microprocessor and several peripherals on a single chip. It's intended for use in controllers, instrumentation and other embedded applications. The 80188 is identical to the 80186 except for its eight-bit external data bus.

Features

Enhanced 8086
Up to 20-MHz clock
1M addressing ability
Clock generator
Two DMA channels
Programmable interrupt controller
Three programmable 16-bit timers
Programmable memory and chip-select logic
Programmable wait-state generator
Local-bus controller
Object-code-compatible with 8086/8
Ten added instruction types

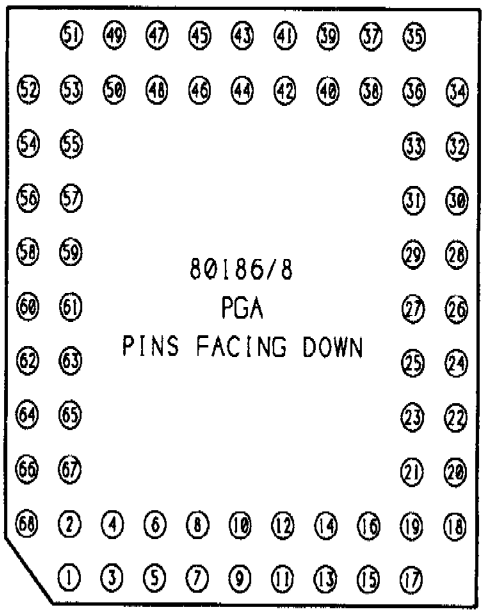
Related chips

80C186XL is low power, 20-MHz clock.
80C186EA has power-save modes, 20-MHz clock.
80C186EB has two serial channels, power-save modes, 16 port pins, 20-MHz clock.
80C186EC has two serial channels, power-save modes, four DMA channels, watchdog timer, 24 port pins, 16-MHz clock.



COMPUTERCRAFT / *August 1993*

80188 has A8-A15 in place of AD8-AD15.



Pin functions are the same as for PLCC.

Signal	Pin(s)	Type	Function
AD0-AD7	2,4,6,8,11,13,15,17	I/O	Low Address/Data Bus
AD8-AD15	1,3,5,7,10,12,14,16	I/O	High Address/Data Bus (80186 Only)
A8-A15	1,3,5,7,10,12,14,16	Output	High Address Bus (80188 Only)
A16/S3	68	Output	Address Bit 16/Bus Cycle Status 3
A17/S4	67	Output	Address Bit 17/Bus Cycle Status 4
A18/S5	66	Output	Address Bit 18/Bus Cycle status 5
A19/S6	65	Output	Address Bit 19/Bus Cycle status 6
ALE/QS0	61	Output	Address Latch Enable/Queue Status 0
ARDY	55	Input	Asynchronous Ready
-BHE/S7	64	Output	Bus High Enable/Bus Cycle Status 7
CLKOUT	56	Output	Clock Output
-DEN	39	Output	Data Enable
DRQ0	18	Input	DMA Request Channel 0
DRQ1	19	Input	DMA Request Channel 1
DT/-R	40	Output	Data Transmit/Receive
HOLD	50	Input	Bus Hold
HOLDA	51	Output	Bus Hold Acknowledge
INT0	45	Input	Interrupt request 0
INT1/SELECT	44	Input	Interrupt Request 1/Save Select
INT2/-INTA0	42	I/O	Interrupt Request 2/Acknowledge 0
INT3/-INTA1/IRQ	41	I/O	Interrupt Request 3/Acknowledge 1/Slave Request
-LCS	33	Output	Lower Memory Chip Select
-LOCK	48	Output	Bus Lock
-MCS0	38	Output	Midrange Memory Chip Select 0
-MCS1	37	Output	Midrange Memory Chip Select 1
-MCS2	36	Output	Midrange Memory Chip Select 2
-MCS3	35	Output	Midrange Memory Chip Select 3
NMI	46	Input	Nonmaskable Interrupt request
-PCS0	25	Output	Peripheral Chip Select 0
-PCS1	27	Output	Peripheral Chip Select 1
-PCS2	28	Output	Peripheral Chip Select 2
-PCS3	29	Output	Peripheral Chip Select 3
-PCS4	30	Output	Peripheral Chip Select 4
-PCS5/A1	31	Output	Peripheral Chip Select 5/Latched A1
-PCS6/A2	32	Output	Peripheral Chip Select 6/Latched A2
-RD/-QSMD	62	I/O	Read Strobe/Queue Status Mode
-RES	24	Input	CPU Reset
RESET	57	Output	Reset Output
-S0	52	Output	Bus Cycle Status 0
-S1	53	Output	Bus Cycle Status 1
-S2	54	Output	Bus Cycle Status 2
SRDY	49	Input	Synchronous Ready
-TEST	47	I/O	Wait Instruction Continues if Low
TMR IN 0	20	Input	Timer Input 0
TMR IN 1	21	Input	Timer Input 1
TMR OUT 0	22	Output	Timer Output 0
TMR OUT 1	23	Output	Timer Output 1
-UCS	34	Output	Upper Memory Chip Select
-WR/QS1	63	Output	Write Strobe/Queue Status 1
Vcc	9,43	Input	Power Supply (+5V)
Vss	26,60	Input	System Ground
X1	59	Input	Crystal 1
X2	58	Output	Crystal 2

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Corrections

March 1993 Disk Drive Interfaces section transpose the two cable drawings on the first page with those on the second page.

ComputerCraft Magazine's PC Connector Guide

With this issue, *ComputerCraft* launches a series of pull-outs that contain useful and important data tables and other information germane to helping readers understand, troubleshoot and repair their PC and compatible computers. Much of the material contained in these pull-outs will be in tabular form, as is the case with this first offering. In later pull-outs, we'll supplement tabular data with how-to drawings and caption text on such diverse subjects as installing hard and floppy-disk drives, replacing and setting up a motherboard and building your own PC-compatible computer from scratch.

Prepared by TJ Byers. Copyright 1993 CQ Communications, Inc.,
76 North Broadway, Hicksville, NY 11801.

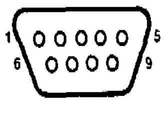
Serial Ports

RS-232C Serial PC Modem Port

Nine-Pin D-Shell Connector

Pin	Function	Signal Description
1	I	Data Carrier detect (DCD)
2	I	Receive Data (RX)
3	O	Transmit Data (TX)
4	O	Data Terminal Ready (DTR)
5	GND	Signal Ground
6	I	Data Set Ready (DSR)
7	O	Request To Send (RTS)
8	I	Clear To Send (CTS)
9	I	Ring Indicator (RI)

With introduction of the PC AT in 1984, IBM redefined the RS-232C serial port by packing the nine modem signal lines into a nine-pin connector.

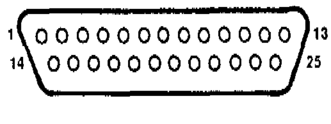


RS-232C Serial PC Modem Port

25-Pin D-Shell Connector

Pin	Function	Signal Description
1	GND	Earth Ground
2	O	Transmit Data (TX)
3	I	Receive Data (RX)
4	O	Request To Send (RTS)
5	I	Clear To Send (CTS)
6	I	Data Set Ready (DSR)
7	GND	Signal Ground (GND)
8	I	Data Carrier Detect (DCD)
20	O	Data Terminal Ready (DTR)
22	I	Ring Indicator (RI)

Modem version of the RS-232C interface uses only nine signal lines of the original IEEE 25-pin definition.

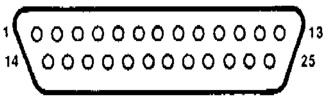


RS-232C Serial Port

25-Pin D-Shell Connector

Pin	Function	Signal Description
1	GND	Earth Ground
2	O	Transmit Data (TXD)
3	I	Receive Data (RXD)
4	O	Request To Send (RTS)
5	I	Clear To Send (CTS)
6	I	Data Set Ready (DSR)
7	GND	Signal Ground (GND)
8	I	Data Carrier Detect (DCD)
9	O	+12 Volts
10	O	−12 Volts
11	N.A.	Reserved
12	I	Secondary Line Signal Detector
13	I	Secondary Clear To Send
14	O	Secondary Transmit Data
15	O	DCE Transmitter Signal Timing
16	I	Secondary Receive Data
17	I	Receiver Signal Timing
18	N.A	Not Used
19	O	Secondary Request To Send
20	O	Data Terminal Ready (DTR)
21	I	Signal Quality Detector
22	I	Ring Indicator
23	O	Data Rate Selector (DRS)(V.24)
24	O	DTE Transmitter Signal Timing
25	N.A.	Reserved

The bidirectional RS-232C serial port, as defined by the IEEE standard, makes full use of the 25-pin connector.

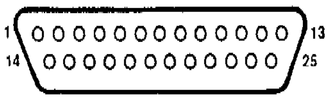


RS-423 Serial Port

25-Pin D-Shell Connector

Pin	Function	Signal Description
1	GND	Earth Ground (Shield)
2	O	Send Data (SD)
3	I	Receive Data (RD)
4	O	Request To Send (RS)
5	I	Clear To Send (CS)
6	I	Data Mode (DM)
7	GND	Signal Ground (SG)
8	I	Receiver Ready (RR)
9	N.A.	Not Defined
10	N.A.	Not Defined
11	N.A.	Reserved
12	I	Signal Rate Indicator (SI)
13	N.A.	Not Defined
14	N.A.	Not Defined
15	O	Send Signal Timing (ST)
16	N.A.	Not Defined
17	I	Receive Timing (RT)
18	O	New Signal (NS)
19	N.A.	Not Defined
20	O	Terminal Ready (TR)
21	I	Signal Quality (SQ)
22	I	Incoming Call (IC)
23	O	Select Frequency/Select Rate (SF/SR)
24	O	Terminal Timing (TT)
25	I	Terminal In Service (TI)

Essentially, the 25-pin RS-423 port defined by RS-449 is a faster version of the popular RS-232C port. At speeds up to 19,200 bps, it plugs directly into an RS-232C port.

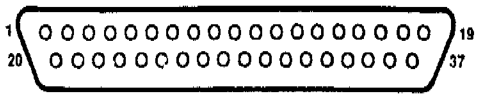


RS-422 Serial Port

37-Pin D-Shell Connector

Pin	Function	Signal Description
1	GND	Earth Ground
2	I	Signal Rate Indicator
3	N.A.	Spare
4	O	Send Data (SD)
5	O	Send Timing (ST)
6	I	Receive Data (RD)
7	O	Request To Send (RTS)
8	I	Receive Timing (RT)
9	I	Clear To Send (CTS)
10	O	Local Loopback (LL)
11	I	Data Mode (DM)
12	O	Terminal Ready (TR)
13	I	Receiver Ready (RR)
14	O	Remote Loopback (RL)
15	I	Incoming Call (IC)
16	O	Select Frequency/Select Rate (SF/SR)
17	O	Terminal Timing (TT)
18	I	Test Mode (TM)
19	GND	Ground
20	GND	Receive Twisted-Pair Common (RC)
21	GND	Spare Twisted-Pair Return
22	GND	Send Data Twisted-Pair Return (−SD)
23	GND	Send Timing Twisted-Pair Return
24	GND	Receive Data Twisted-Pair Return
25	GND	Request To Send Twisted-Pair Return (−RS)
26	GND	Receive Timing Twisted-Pair Return (−RT)
27	GND	Clear To Send Twisted-Pair Return (−CS)
28	I	Terminal In Service (IS)
29	GND	Data Mode Twisted-Pair Return (−DM)
30	GND	Terminal Ready Twisted-Pair Return (−TR)
31	GND	Receiver Twisted-Pair Return (−RR)
32	O	Select Standby (SS)
33	I	Signal Quality (SQ)
34	O	New Signal (NS)
35	GND	Terminal Timing Twisted-Pair Return (−TT)
36	I	Standby Indicator (SB)
37	GND	Send Twisted-Pair Common (SC)

The 37-pin RS-422 port, defined by RS-449 standard, is a differential serial interface well-suited for instrumentation use. Because it uses differential signal techniques, it can send data at faster baud rates over longer distances than the RS-232C interface.



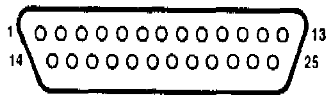
Printer Ports

Parallel Printer Port

25-pin D-shell Connector

Pin	Function	Signal Description
1	I/O	−Strobe D0
2	I/O	Data Bit 0 (PRTD0)
3	I/O	Data Bit 1 (PRTD1)
4	I/O	Data Bit 2 (PRTD2)
5	I/O	Data Bit 3 (PRTD3)
6	I/O	Data Bit 4 (PRTD4)
7	I/O	Data Bit 5 (PRTD5)
8	I/O	Data Bit 6 (PRTD6)
9	I/O	Data Bit 7 (PRTD7)
10	I	−Acknowledge (ACK) D6
11	I	Busy D7 I
12	I	Paper End/Empty (PE) D5
13	I	Select (SLCT) D4
14	O	−Auto Feed (AUTOFDXT) D1
15	O	−Error/Oscillator
16	O	−Initialize Printer (INIT) D2
17	O	−Select Input (SLCTIN) D3
18-25	GND	Ground

The original printer port, as supported by the IBM PC and IBM XT, is a unidirectional interface that only outputs data. In the PC AT and its 386/486 clones, the data lines are bidirectional.

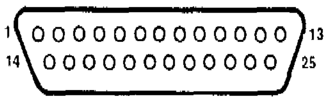


Serial Printer Port

25-Pin D-Shell Connector

Pin	Function	Signal Description
1	GND	Earth Ground
2	O	Transmit Data (TXD)
3	I	Receive Data (RXD)
6	I	Data Set Ready (DSR)
7	GND	Signal Ground (GND)
8	I	Data Carrier Detect (DCD)
11	O	Reverse Channel
17	O	TTY Transmit Data (TTY-TXD)
20	O	Data Terminal Ready (DTR)
23	O	TTY Receive Data Return
24	I	TTY Transmit Data Return
25	I	TTY Receive Data (TTY-RXD)
4,5,9,10,12,13,14,15,16,18,19,21,22		Not Connected

25-pin serial printer port is similar to RS-232C serial port in many ways and can often be used interchangeably. Except for TTY-TXD and TTY-RXD, all signals are based on RS-232C voltage levels.

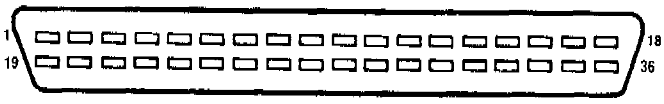


Centronics Printer Connector

36-Pin Amphenol Connector

Pin	Function	Signal Description	Pin	Function	Signal Description
1	I	Strobe	19	GND	Strobe Twisted-Pair Return
2	I	Data Bit 0	20	GND	Data Bit 0 Twisted-Pair Return
3	I	Data Bit 1	21	GND	Data Bit 1 Twisted-Pair Return
4	I	Data Bit 2	22	GND	Data Bit 2 Twisted-Pair Return
5	I	Data Bit 3	23	GND	Data Bit 3 Twisted-Pair Return
6	I	Data Bit 4	24	GND	Data Bit 4 Twisted-Pair Return
7	I	Data Bit 5	25	GND	Data Bit 5 Twisted-Pair Return
8	I	Data Bit 6	26	GND	Data Bit 6 Twisted-Pair Return
9	I	Data Bit 7	27	GND	Data Bit 7 Twisted-Pair Return
10	O	Acknowledge (ACKNLG)	28	GND	Acknowledge Twisted-Pair Return
11	O	Busy	29	GND	Busy Twisted-Pair Return
12	O	Paper End/Empty (PE)	30	GND	Paper End/Empty Twisted-Pair Return
13	O	Logic High ('5 Volts)	31	I	−Initialize (INIT)
14	I	Auto Feed XT	32	O	−Error
15	N.A.	Not Used	33	GND	Signal Ground (Connects 19-30 to GND)
16	GND	Logic Ground	34	N.A.	Not Used
17	GND	Earth Ground	35	O	Logic High (+5 Volts)
18	N.A.	Not Used	36	I	−Select Input (SLCT IN)

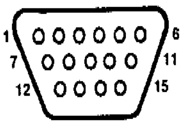
The 36-pin Centronics printer cable uses twisted-pair data and control lines to minimize crosstalk and outside interference. Pins 13 and 35 can be used for printer-detect lines or low-current power sources.



Video Interfaces

VGA Color

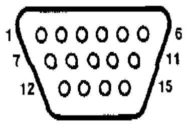
15-Pin Miniature D-Shell Connector

Pin	Signal	
1	Red Video	
2	Green Video	
3	Blue Video	
4	Monitor ID Bit 2	
5	Ground	
6	Red Video Ground	
7	Green Video Ground	
8	Blue Video Ground	
9	No Connection	
10	Sync Ground	
11	Monitor ID Bit 0	
12	Monitor ID Bit 1	
13	Horizontal Sync	
14	Vertical Sync	
15	No Connection	

The 15-pin video interface supports both VGA and super-VGA video signals. Polarity of the horizontal and vertical sync pulses determines screen resolution.

VGA Monochrome

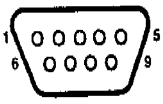
15-Pin Miniature D-Shell Connector

Pin	Signal	
1	Not Used	
2	Monochrome Video	
3	Not Used	
4	Not Used	
5	Ground	
6	Key	
7	Monochrome Ground	
8	Not Used	
9	No Connection	
10	Horizontal Sync Ground	
11	Not Used	
12	Vertical Sync Ground	
13	Horizontal Sync	
14	Vertical Sync	
15	No Connection	

The video controller board senses the presence of a monochrome monitor by the absence of the Monitor ID bits. Like color VGA, video signal is analog, with 0.7-volt gray-scale (color) saturation level.

EGA/CGA Color

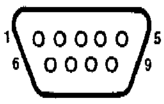
Nine-Pin D-Shell Connector

Pin	Signal	
1	Red Video	
2	Green Video	
3	Blue Video	
4	Horizontal Sync	
5	Vertical Sync	
6	Red Video Ground	
7	Green Video Ground	
8	Blue Video Ground	
9	Ground	

The nine-pin video connector is basically a digital interface used for CGA and EGA video graphics. However, many multisync monitors can support both analog and digital video modes through this nine-pin interface.

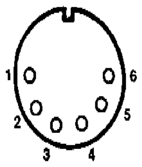
Mouse Ports

Nine-Pin D-Shell Connector

Pin	Signal	
1	Not Used	
2	Data	
3	Clock	
4	+5 Volts	
5	Ground	
6	Not Used	
7	Enable Mouse	
8	Mouse Ready	
9	Not Used	

The nine-pin serial-port mouse uniquely uses two of the serial port's data control lines to let software applications know when the mouse is present.

Six-Pin Miniature DIN Connector

Pin	Signal Description	
1	Data	
2	Not Used	
3	Signal Ground	
4	+5 Volts	
5	Clock	
6	Not Used	
Shell	Earth Ground	

Originally designed for notebook use, the six-pin miniature DIN mouse connector is finding widespread use in small-foot-print desktop PCs—and video boards from ATI and Sota.

ComputerCraft Magazine's PC Connector Guide

This is the third in a series of pull-outs that contain useful and important data tables and other information germane to helping readers understand, troubleshoot and repair personal computers, single-board computers and microcontrollers. In earlier issues, we focused on Serial, Parallel and Printer Ports, Video Interfaces, Mouse Ports, Floppy- and Hard-Disk Drive Interfaces and SCSI Interfaces. This time around, we provide a potpourri of Local-Area Network, Power-Supply MIDI Interface and Adapter connection details.

Prepared By TJ Byers Copyright 1992 by CQ Communications, Inc.
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Local-Area Network

Ethernet Twisted-Pair (Hub to PC)

Eight-Pin RJ-45 Phone Plug

Hub End Pin	Conductor Color	PC End Pin	Signal Description
1	Wht/Org	1	Receive+ to Transmit+
2	Org/Wht	2	Receive- to Transmit-
3	Wht/Grn	3	Transmit+ to Receive+
6	Grn/Wht	6	Transmit- to Receive-

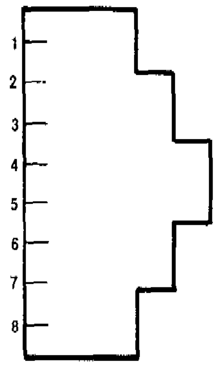
Twisted-pair Ethernet link uses common telephone wire and RJ-45 connectors. Notice wiring differences between Hub-to-PC and Hub-to-Hub links.

Ethernet Twisted-Pair (Hub to Hub)

Eight-Pin RJ45 Phone Plug

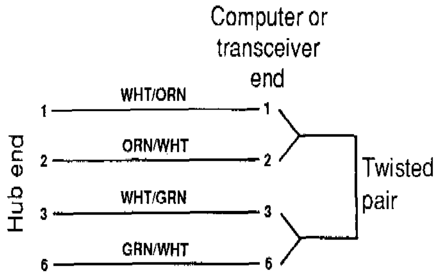
Hub1 End Pin	Conductor Color	Hub2 End Pin	Signal Description
1	White/Org	6	Receive+ To Transmit-
2	Org/White	3	Receive- To Transmit+
3	White/Grn	2	Transmit+ To Receive-
6	Grn/White	1	Transmit- To Receive+

Twisted-pair Ethernet link uses common telephone wire and RJ-45 connectors. Notice Wiring differences between Hub-to-PC and Hub-to-Hub links.

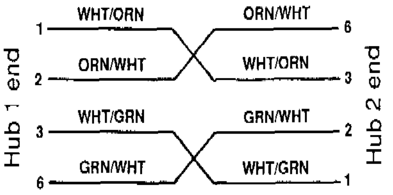


RJ-45

White/Orange (WHT/ORN) = Receive +; Orange/White (ORN/WHT) = Receive –
White/Green (WHT/GRN) = Transmit +; Green/White (GRN/WHT) = Transmit –



STRAIGHT-THROUGH CABLE



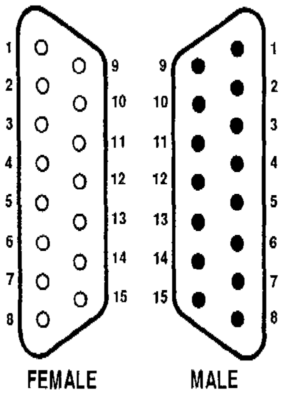
CROSSOVER CABLE

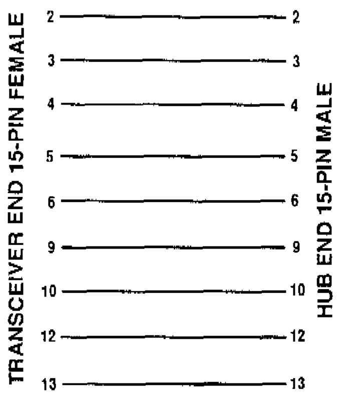
Thick Ethernet AUI Connector

15-Pin D-Shell Connector

Pin	Signal
1	Collision Shield
2	Collision+
3	Transmit+
4	Receive Shield
5	Receive+
6	Power Return
7	Not Used
8	Not Used
9	Collision-
10	Transmit-
11	Transmit Shield
12	Receive-
13	+12 Volts
14	Voltage Shield
15	Not Used

Thick Ethernet interface uses shielded twisted pairs to increase cable and Ethernet link length. It uses 15-pin AUI connector identical to 15-pin D-shell connector used by Game and MIDI ports.





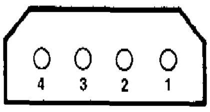
Power-Supply Connections

Disk-Drive Power Source

Four-Pin Polarized Plastic Connector
Both Large and Small

Pin	Assignment	Conductor Color
1	+12 Volts	Yel/Blu/Org
2	+12-Volt Ground	Blk
3	+5-Volt Ground	Blk
4	+5 Volts	Red

Both +12 and +5 volts are available from four-pin isk-drive connector. Power connector comes in two sizes, one for standard 5¼" and smaller one for 3½" drives, but pinouts are same.



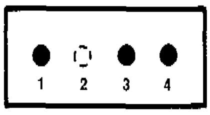
1 = -12V
2 = 12V dc ground
3 = +5V
4 = 5V dc ground

Backup Battery Connector

Four-Pin In-Line Berg Connector

Pin	Assignment	Conductor Color
1	+ Battery	Red
2	Key (Pin Missing)	N.A.
3	Ground	Black
4	Ground	Black

While backup battery can take many forms, it interfaces to motherboard via a common connector. If there is no alignment key, mate red conductor with +battery pin on motherboard.



1 = -V
2 = Key
(no connection)
3, 4 = Ground

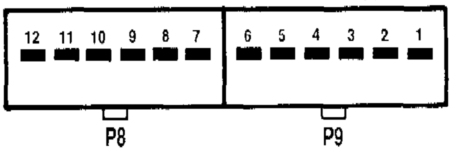
Motherboard Power Source

Dual Six-Pin In-Line Plastic Connectors

Pin	Assignment	Conductor Color
1	Good Power Sense	Wht/Org
2	+5 Volts	Red
3	+12 Volts	Blu
4	-12 Volts	Wht/Blu
5	Ground	Blk
6	Ground	Blk
7	Ground	Blk
8	Ground	Blk
9	-5 Volts	Org
10	+5 Volts	Red
11	+5 Volts	Red
12	+5 Volts	Red

Power is supplied to motherboard via two heavy-duty, six-pin plastic connectors. Black wires are always in middle. Connectors are keyed to a slot that forces them to be folded back at top of slot when inserting or removing them.

See motherboard for connector type



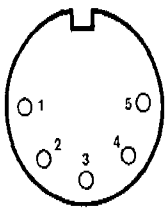
1 = Power ground (WHT/ORN)
2 = +5V (RED)
3 = +12V (BLUE)
4 = -12V (WHT/BLK)
5, 6, 7, 8 = Ground (BLK)
9 = -5V (ORN)
10, 11, 12 = +5V (RED)

MIDI Interface

MIDI Input

Five-Pin DIN Connector

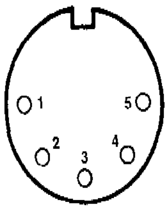
Pin	Signal
1	Not Used
2	Not Used
3	Not Used
4	Signal Ground
5	Signal Input



MIDI Through

Five-Pin DIN Connector

Pin	Signal
1	Not Used
2	Shield
3	Not Used
4	+5 Volts
5	Signal Out

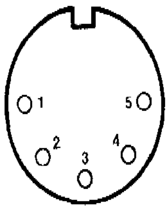


MIDI Output

Five-Pin DIN Connector

Pin	Signal
1	Not Used
2	Shield
3	Not Used
4	+5 Volts
5	Signal Out

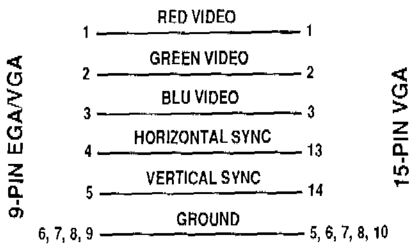
Five-pin DIN high-quality audio connector is type of choice for MIDI interface. It comes in three versions: input, output and optional throughput.



Adapters

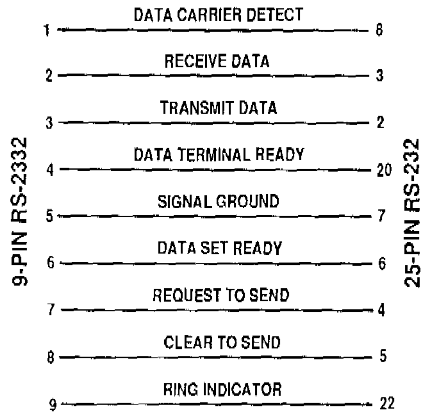
Nine-Pin EGA/VGA To 15-Pin VGA

Nine-Pin	Signal	15 Pin
1	Red Video	1
2	Green Video	2
3	Blue Video	3
4	Horizontal Sync.	13
5	Vertical Sync.	14
6,7,8,9	Ground	5,6,7,8,10
None	No Connection	4,9,11,12,15



Nine-Pin To 25-Pin RS-232C

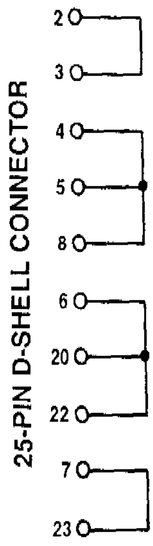
Nine-Pin	Signal	25-Pin
1	Data Carrier Detect	8
2	Receive Data	3
3	Transmit Data	2
4	Data Terminal Ready	20
5	Signal Ground	7
6	Data Set Ready	6
7	Request To Send	4
8	Clear To Send	5
9	Ring Indicator	22



25-Pin RS-232C Null Modem

25-pin D-Shell Connector

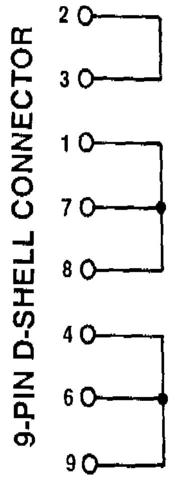
Pin 2 To Pin 3
Pin 4 To Pin 5 To Pin 8
Pin 6 To Pin 20 To Pin 22
Pin 7 To Pin 23



Nine-Pin RS-232C Null Modem

Nine-Pin D-Shell Connector

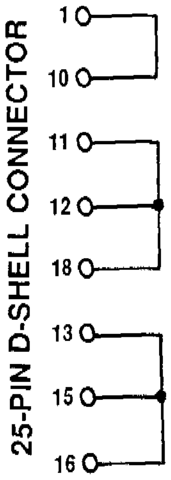
Pin 2 To Pin 3
Pin 1 To Pin 7 To Pin 8
Pin 4 To Pin 6 To Pin 9



25-Pin Null Printer

25-Pin D-Shell Connector

Pin 1 To Pin 10
Pin 11 To Pin 12 To Pin 18
Pin 13 To Pin 15 To Pin 16



RJ-11 Telephone Jack

Pin	Conductor	Signal
1	Yellow	Line 2 Tip
2	Green	Line 1 Ring
3	Red	Line 1 Tip
4	Black	Line Ring

Troubleshooting an RJ-11 telephone connection is as simple as measuring voltages across red/green (Line 1) or yellow/black (Line 2) conductors. On-hook measures about 48 volts dc, off-hook about 20 volts dc and ring signal is 100 volts ac (enough to light both electrodes of an NE-2 lamp through a 22K resistor.

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ComputerCraft Magazine's Connector Guide

This is the second in a continuing series of pull-outs that contain important and often hard-to-find data needed for understanding, maintaining, troubleshooting and repairing IBM PC and compatible computers ranging from the initial 8088-based PC to the latest-technology systems now in use. The first pull-out, which appeared last month in the February issue, provided tabular listings and pinout drawings for Serial, Printer and Mouse Ports and Video Interfaces. This time around, we focus on floppy-, hard-disk and SCSI interfaces.

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Disk-Drive Interfaces

Floppy and Hard Disk-Drive Interfaces

Floppy-Disk Drive A Interface

(34-Pin Edge Connector)

Pin	Signal	Signal Description
2	RPM/LC	Speed Select For Two-Speed Drives
4	N.A.	Not Used
5	Key	Missing Pin
6	N.A.	Not Used
8	INDEX	-Track Index
[10	MOTOR0	-Motor Enable Drive 0]
[12	FDSEL1	-Floppy Drive Select 1]
[14	FDSEL0	-Floppy Drive Select 0]
[16	MOTOR1	-Motor Enable Drive 1]
18	DIR	Direction
20	STEP	-Step
22	WDATA	-Write Data
24	WE	-Write Enable
26	TRK0	-Track 0
28	WP	-Write Protect
30	RDATA	-Read Data
32	HDSEL	Head Select
34	DSKCHNG	Diskette Change
1,3,7,9,11,13,15,17,19,21,23,25,27,29,31,33 Go To Ground		

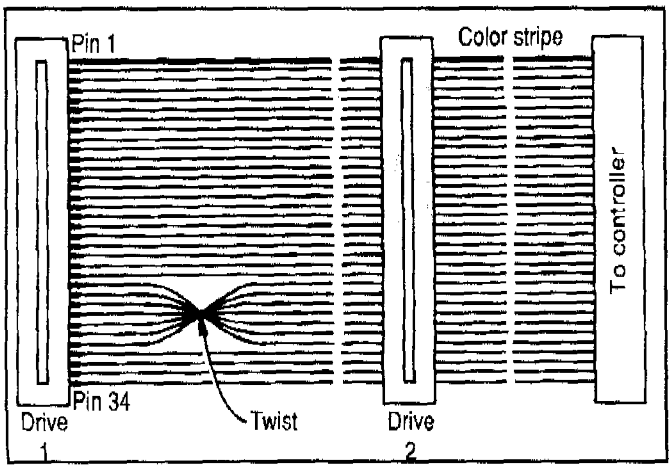
Single cable with two printed-circuit board edge connectors services both A and B floppy drives. Twist in cable changes pinout of control signals, making it simple to activate desired drive without affecting the other.

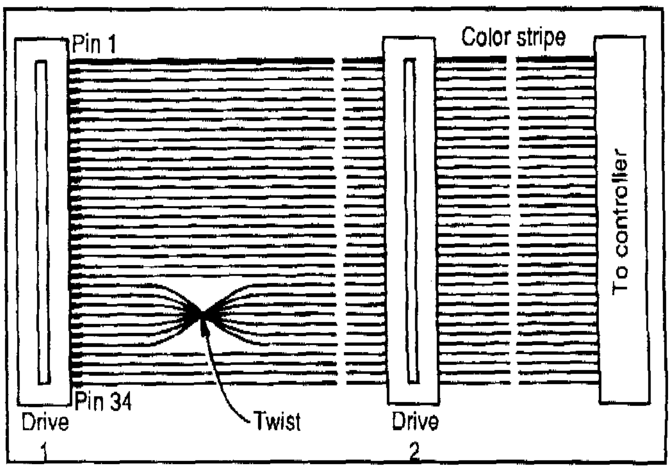
Floppy-Disk Drive B Interface

(34-Pin Edge Connector)

Pin	Signal	Signal Description
2	RPM/LC	Speed Select For Two-Speed Drives
4	N.A.	Not Used
5	Key	Missing Pin
6	N.A.	Not Used
8	INDEX	-Track Index
[10	MOTOR1	-Motor Enable Drive 1]
[12	FDSEL0	-Floppy Drive Select 0]
[14	FDSEL1	-Floppy Drive Select 1]
[16	MOTOR0	-Motor Enable Drive 0]
18	DIR	Direction
20	STEP	-Step
22	WDATA	-Write Data
24	WE	-Write Enable
26	TRK0	-Track 0
28	WP	-Write Protect
30	RDATA	-Read Data
32	HDSEL	Head Select
34	DSKCHNG	Diskette Change
1,3,7,9,11,13,15,17,19,21,23,25,27,29,31,33 Go To Ground		

Single cable with two printed-circuit board edge connectors services both A and B floppy drives. Twist in cable changes pinout of control signals, making it simple to activate desired drive without affecting the other.



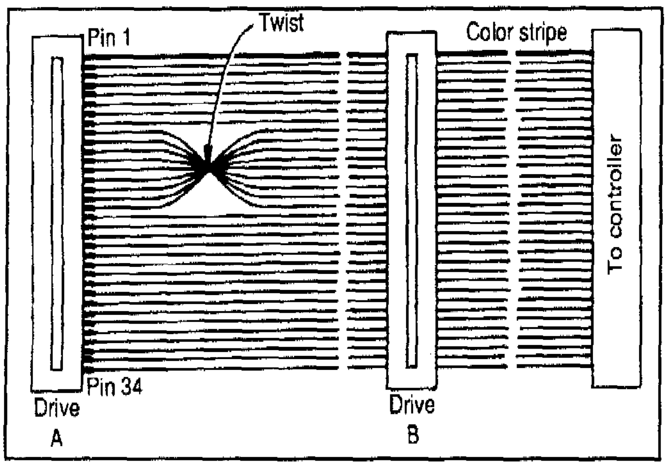


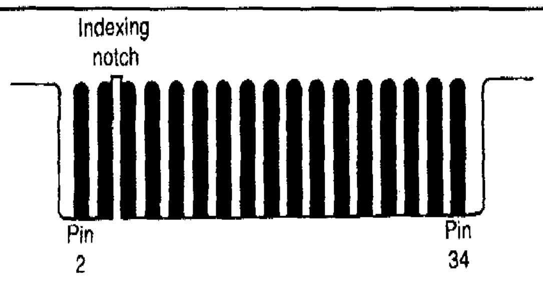
ST-506/412 Hard-Disk Drive Interface

(34-Pin Control-Cable Edge Connector)

Pin	I/O Status	Signal Description
1	I	–Head Select 8
3	I	–Head Select 4
5	I	–Write Gate
7	O	–Seek Complete
9	O	–Track 0
11	O	–Write Fault
13	I	–Head Select 1
15	N.A.	To Data Cable Pin 7
17	I	–Head Select 2
19	O	–Index
21	O	–Ready
23	I	–Step
25	I	–Drive Select 1
27	I	–Drive Select 2
29	I	–Drive Select 3
31	I	–Drive Select 4
33	I	–Direction In
2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34 Go To Ground		

ST-506/412 hard-disk drives interface to controller via 34-pin control and 20-pin data cables. Like floppy drives, twist in 34-pin cable changes control-signal pinouts so that two drives can be controlled from single cable. However, twisted area is wider, making floppy-drive and ST-506/412 cables non-interchangeable, though ST-506/412 cables are interchangeable with ESDI cables.





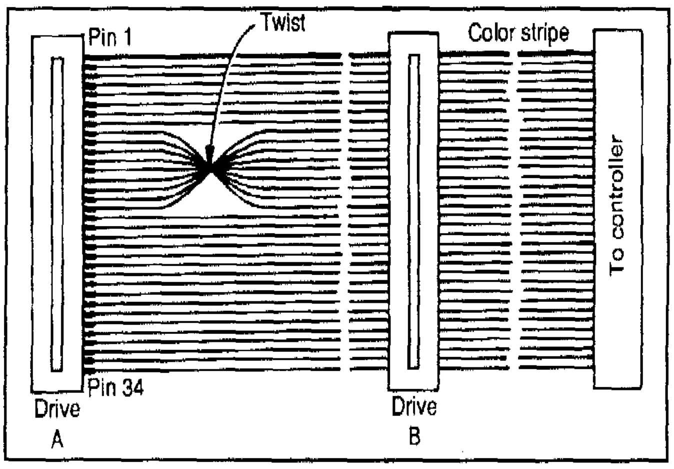
NOTE:
All odd-numbered pins are on reverse side.

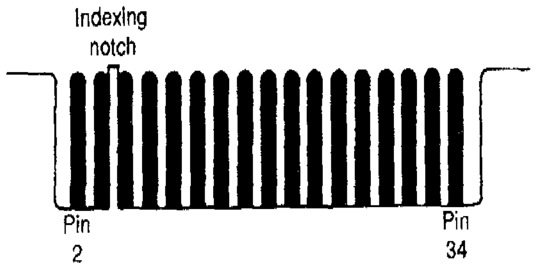
ESDI Hard-Disk Drive Interface

(34-Pin Control-Cable Edge Connector)

Pin	I/O Status	Signal Description
1	I	–Head Select 3
3	I	–Head Select 2
5	I	–Write Gate
7	O	–Configure/Status Data
9	O	–Transfer Acknowledge
11	I	–Attention
13	I	–Head Select 0
15	O	–Sector/Address Mark Found
17	I	–Head Select 1
19	O	–Index
21	O	–Ready
23	I	–Transfer Request
25	I	–Drive Select 0
27	I	–Drive Select 1
29	I	–Drive Select 2
31	I	–Read Gate
33	I	–Command Data
2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34 Go To Ground		

ESDI hard-disk drives interface to controller via 34-pin control and 20-pin data cables. Like floppy drives, a twist in 34-pin cable changes pinout of control signals so that two drives can be controlled from single cable. However, twisted area is wider, making floppy and ESDI cables non-interchangeable. ESDI and ST506/412 cables are interchangeable.



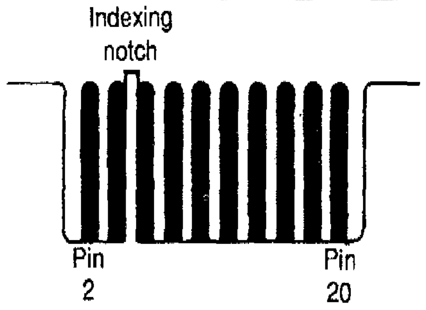


NOTE:
All odd-numbered pins are on reverse side.

ST-506/412 Hard-Disk Drive Interface

(20-Pin Data-Cable Edge Connector)

Pin	Signal Description
1	Drive Selected
3	Reserved
5	Reserved
7	To Control Cable Pin 15
9	Reserved
13	+MFM Write Data
14	–MFM Write Data (MFM Write Signal Return Line)
17	+MFM Read Data
18	–MFM Read Data (MFM Read Signal Return Line)
2,4,6,8,9,10,11,12,14,15,16,19,20 Go To Ground	



NOTE:
All odd-numbered pins are on reverse side.

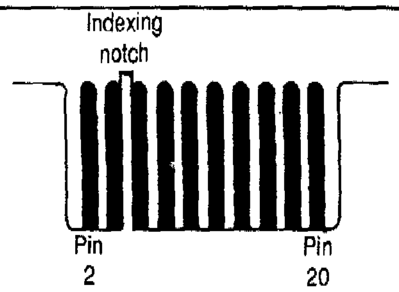
See note at end of ST-506/412 Hard-Disk Interface control-cable table for details.

ESDI Hard-Disk Drive Interface

(20-Pin Data-Cable Edge Connector)

Pin	Signal Description
1	–Drive Selected
2	-Sector/Address Mark Found
3	–Command Complete
4	–Address Mark Enable
5	Step Mode (Reserved)
7	–Write Clock Return Line
8	+Write Clock
9	Cartridge Changed
10	+Read/Reference Clock
11	–Read/Reference Clock Return Line
13	+NRZ Write Data
14	–NRZ Write Data Return Line
17	+NRZ Read Data
18	–NRZ Read Data Return Line
20	–Index
6,13,15,16,19 Go To Ground	

See note at end of ESDI Hard-Disk Drive Interface for further details.



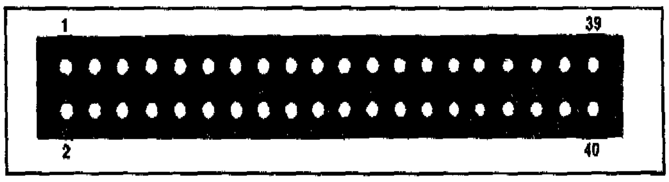
NOTE:
All odd-numbered pins are on reverse side.

IDE Hard-Disk Drive Interface (For PC/XT)

(40-Pin Dual In-Line Berg Connector)

Pin	Signal	Signal Description
1	Reset	-Reset
3		D7 Data Bit 7
5		D6 Data Bit 6
7		D5 Data Bit 5
9		D4 Data Bit 4
11		D3 Data Bit 3
13		D2 Data Bit 2
15		D1 Data Bit 1
17		D0 Data Bit 0
20	Key	Pin Missing
21	AEN	Address Enable
23	IOW	I/O Write Data
25	IOR	I/O Read Data
27	DACK	DMA Acknowledge
29	DRQ	DMA Request
31	IRQ14	Interrupt Request From IDE
33	A1	Address Bit 1
35	A0	Address Bit 0
36	A2	Address Bit 2
37	–CS1FX	Drive Chip Select 0 (1F0 Through 1F7)
39	N.A.	Not Used
2,4,2,8,10,12,14,16,18,19,22,24,26,28,30,32,34,36,38,40 Go To Ground		

Because IDE control electronics is built into drive, no external controller is needed and drive generally just plugs into data lines on motherboard via a single cable. IDE interfaces exist for 16-bit PCs (80286 and later designs) and eight-bit PCs (8086 and 8088).

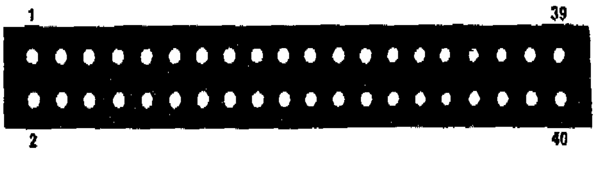


IDE Hard-Disk Drive Interface (For PC/XT)

(40-Pin Dual In-Line Berg Connector)

Pin	Signal	Signal Description
1	RESET	-Reset
3	D7	Data Bit 7
4	D8	Data Bit 8
5	D6	Data Bit 6
6	D9	Data Bit 9
7	D5	Data Bit 5
8	D10	Data Bit 10
9	D4	Data Bit 4
10	D11	Data Bit 11
11	D3	Data Bit 3
12	D12	Data Bit 12
13	D4	Data Bit 4
14	D13	Data Bit 13
15	D1	Data Bit 1
16	D14	Data Bit 14
17	D0	Data Bit 0
18	D15	Data Bit 15
20	KEY	Pin Missing
21	DMARQ	DMA Request
23	IOW	I/O Write Data
25	IOR	I/O Read Data
27	IORDY	I/O Channel Ready
28	ALE	Address Latch Enable
29	DMAC	DMA Acknowledge
31	IRQ14	Interrupt Request From IDE
32	–IOCS16	Current Data Transfer = 16 Bits
33	A1	Address Bit 1
34	PDIAG	Passed Diagnostics
35	A0	Address Bit 0
36	A2	Address Bit 2
37	–CS0	Drive Chip Select 0 (1F0 Through 1F7)
38	-CS1	Drive Chip Select 1 (3F6 Through 3F7)
39	ACTIVE	IDE Drive Active
2,19,22,24,26,30,40 Go To Ground		

See note at end of IDE Hard-Disk Drive Interface (For PC/XT) for more details.



SCSI Ports

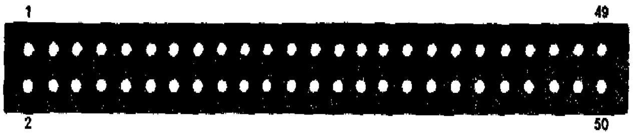
SCSI Single-Ended Interface

(50-Pin Connector, All Versions, Berg Shown)

Pin	Signal	Signal Description
2	DB0	Data Bit 0
4	DB1	Data Bit 1
6	DB2	Data Bit 2
8	DB3	Data Bit 3
10	DB4	Data Bit 4
12	DB5	Data Bit 5
14	DB6	Data Bit 6
16	DB7	Data Bit 7
18	DBP	Parity
25	N.A.	Not Used
26	TEMPWR	Terminator Power
32	ATN	Attention
36	BSY	Busy
38	ACK	Acknowledge
40	RST	Reset
42	MSG	Message
44	SEL	Select
46	C/D	C/D
48	REQ	Request
50	I/O	Input/Output

1,3,5,7,9,11,13,15,17,19,20,21,22,23,24,25,27,28,29,30,31,33,34,35,37,39,41,43,47,49 Go To Ground

Single-Ended SCSI cable can stretch up to 20 feet in length, while differential SCSI cable can reach lengths of 75 feet. Pinout numbering is same for all three different SCSI connectors.



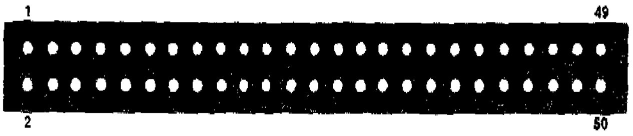
SCSI Differential Interface

(50-Pin Connector, All Versions, Berg Shown)

Pin	Signal	Signal Description
1	SG	Earth Ground (Shield Ground)
2	GND	Ground
3	+DB0	Data Bit 0
4	–DB0	Data Bit 0 Twistted-Pair Return
5	+DB1	Data Bit 1
6	–DB1	Data Bit 1 Twisted-Pair Return
7	+DB2	Data Bit 2
8	–DB2	Data Bit 2 Twisted-Pair Return
9	+DB3	Data Bit 3
10	–DB3	Data Bit 3 Twisted-Pair Return
11	+DB4	Data Bit 4
12	–DB4	Data Bit 4 Twisted-Pair Return
13	+DB5	Data Bit 5
14	–DB5	Data Bit 5 Twisted-Pair Return
15	+DB6	Data Bit 6
16	–DB6	Data Bit 6 Twisted-Pair Return
17	+DB7	Data Bit 7
18	–FB7	Data Bit 7 Twisted-Pair Return
19	+DBP	Parity
20	–DBP	Parity Twisted-Pair Return
21	DIFFSENS	Differential Sense
25	TERMPWR	Terminator Power
26	TERMPWR	Terminator Power
29	+ATN	Attention
30	-ATN	Attention Twisted-Pair Return
33	+BSY	Busy
34	–BSY	Busy Twisted-Pair Return
35	+ACK	Acknowledge
36	–ACK	Acknowledge Twisted-Pair Return
37	+RESET	Reset
38	–RESET	Reset Twisted-Pair Return
39	+MSG	Message
40	–MSG	Message Twisted-Pair Return
41	+SEL	Select
42	–SEL	Select Twisted-Pair Return
43	+C/D	C/D
44	–C/D	C/D Twisted-Pair Return
45	+REQ	Request
46	–REQ	Request Twisted-Pair Return
47	+I/O	Input/Output
48	–I/O	Input/Output Twisted-Pair Return

22,23,24,27,28,31,32,49,50 Go To Ground

See note at end of SCSI Single-Ended Interface for details.



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